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The analysis of interconnected, high-power DC-DC converters for DC zonal electrical distribution

Langlois, Thomas L

Monterey, California. Naval Postgraduate School

NAVAL POSTGRADUATE SCHOOL
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THESIS

THE ANALYSIS OF INTERCONNECTED, HIGH-POWER DC-DC CONVERTERS FOR DC ZONAL ELECTRICAL DISTRIBUTION

by

Thomas L. Langlois

June 1997

Thesis Advisor: John G. Ciezki

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As the United States Navy progresses into the twenty-first century, new concepts in shipboard electrical power management are being explored. One area of significant interest to the Navy is utilization of a DC Zonal Electrical Distribution System (DC-ZEDS) rather than a traditional AC distribution system. This system employs a network of solid-state power conversion devices to supply shipboard electrical loads from two or more high-voltage DC busses. The interconnection of these power converters stimulates several phenomenological questions and motivates multiple areas for study. Of key interest include interconnection dynamics through transmission lines and how the individual power sections of a DC-ZEDS architecture react under real-world load stresses. The focus of this thesis is to use the Power Electronic Building Block Network Testbed at the Naval Postgraduate School to examine the effects of line inductance and step changes in load on interconnected DC-DC converters. The findings of this research effort indicate that a system of networked buck converters can successfully operate in a DC-ZEDS architecture. In particular, buck converters were found to operate stably and were found to have acceptable transient performance for a variety of load conditions and interconnection topologies.

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THE ANALYSIS OF INTERCONNECTED, HIGH-POWER DC-DC CONVERTERS FOR DC ZONAL ELECTRICAL DISTRIBUTION

Thomas L. Langlois
Captain, United States Marine Corps
B.S., University of Texas at Austin, 1987

Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

As the United States Navy progresses into the twenty-first century, new concepts in shipboard electrical power management are being explored. One area of significant interest to the Navy is utilization of a DC Zonal Electrical Distribution System (DC-ZEDS) rather than a traditional AC distribution system. This system employs a network of solid-state power conversion devices to supply shipboard electrical loads from two or more high-voltage DC busses. The interconnection of these power converters stimulates several phenomenological questions and motivates multiple areas for study. Of key interest include interconnection dynamics through transmission lines and how the individual power sections of a DC-ZEDS architecture react under real-world load stresses. The focus of this thesis is to use the Power Electronic Building Block Network Testbed at the Naval Postgraduate School to examine the effects of line inductance and step changes in load on interconnected DC-DC converters. The findings of this research effort indicate that a system of networked buck converters can successfully operate in a DC-ZEDS architecture. In particular, buck converters were found to operate stably and were found to have acceptable transient performance for a variety of load conditions and interconnection topologies.

TABLE OF CONTENTS

I. INTRODUCTION

A. RESEARCH FOCUS

The purpose of this thesis research is to analyze the performance characteristics of interconnected DC-DC converters within the scope of the future Naval DC electrical power distribution systems[1]. As the Navy searches for new and better ways to improve the performance, reliability, and simplicity of modern warships, basic research into concepts facilitating this goal must be undertaken. In the arena of power distribution systems, a future design has been suggested by several authors. Dade [2] suggests that the primary power transmission lines of the vessel would carry DC electrical power at relatively high-voltage levels. The power from these busses would be distributed throughout the vessel through the use of solid-state power conversion devices. The devices convert the distributed DC voltage level to the DC or AC voltage levels required by the loads. This research will explore the interactions between these solid-state devices under various steady-state and transient loads.

The areas focused on are turn-on/turn-off stresses, transient response and the impact of transmission line inductance on the interconnected devices and their control systems. The introductory concepts of future power systems as well as the research approach and equipment are outlined in the remainder of this chapter. An introduction and operational description of the Power Electronics Building Block Testbed (PEBB Testbed), a testing device designed and built by the Naval Postgraduate School Power Research Group, is provided in Chapter II. In Chapter III a description is presented of the

solid-state conversion device that is the focal point of the research, the buck chopper. In Chapter IV specific experimental procedures and testing conditions used in this research endeavor are outlined. The experimental results and observations are documented in Chapter V. Chapter VI contains a listing of the primary research conclusions and recommended future studies.

B. DC ZONAL ELECTRICAL DISTRIBUTION SYSTEM

An interesting shipboard electrical distribution system is advocated and described by Doerry [3]; it is the DC Zonal Electrical Distribution System (DC ZEDS). This system promotes modularity of design within ships by specifying that there be only main power generation equipment, a port and starboard main power DC bus and all other electrical distribution achieved through the use of DC zones. Figure (1-1) shows the basic topology of a zone within the DC ZEDS architecture. The port and starboard DC busses that supply each zone carry on the order of 1000 V DC (higher voltages are anticipated as semiconductor device capabilities are improved) throughout the ship. A Ship Service Converter Module (SSCM) receives the 1000V DC main bus power and produces a regulated lower DC voltage level for use in Ship Service Inverter Modules (SSIM) and intermediate voltage DC loads. The SSIM converts the DC voltage provided by the SSCM into regulated AC power for use by shipboard AC loads. Additional SSCMs are used to convert the intermediate level DC to a third, lower DC voltage for loads that require an even lower level. A system of steering diodes would be utilized to auctioneer service to vital loads by providing uninterrupted power from either bus.

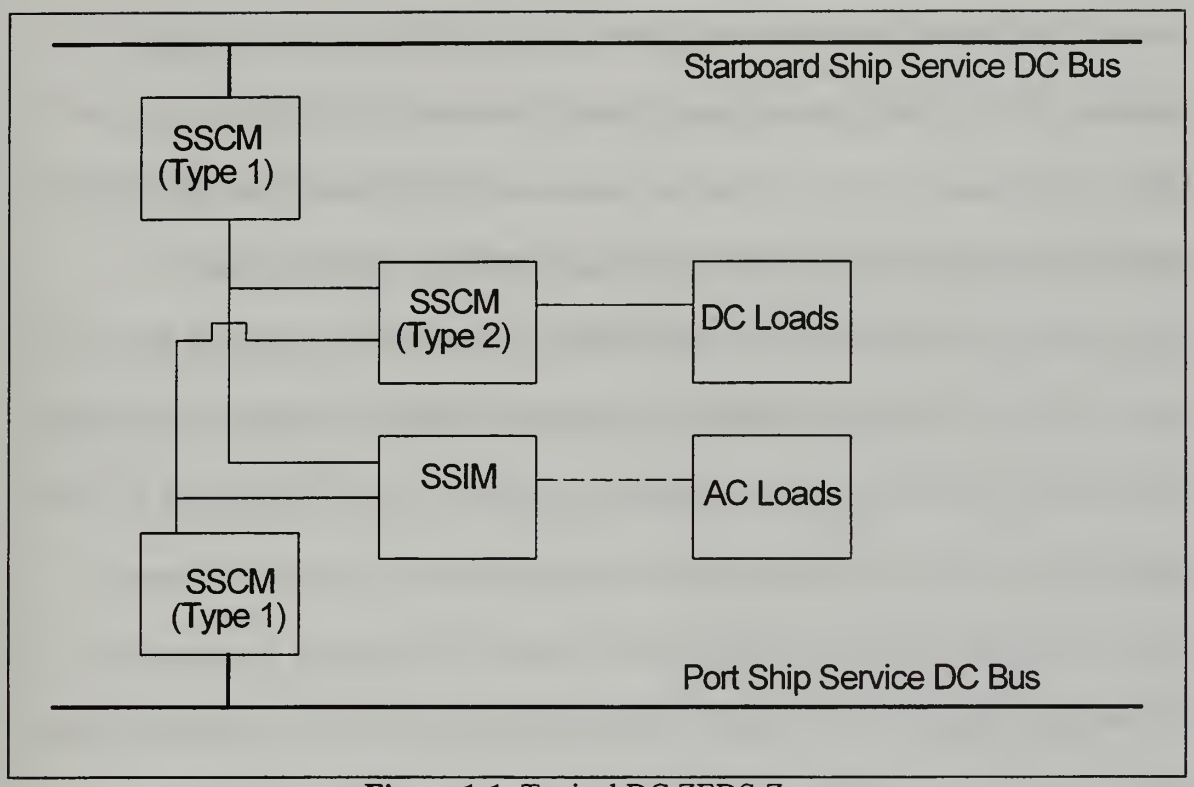

Figure 1-1, Typical DC ZEDS Zone

Figure (1-1) depicts two types of SSCMs, a high voltage to intermediate voltage (Type 1) and intermediate to low voltage (Type 2). There would also be multiple types of SSIMs, each tailored to condition the DC power.differently in order to supply all types of AC loads. The AC outputs of the SSIMs would be at various voltage levels, phase configurations and frequencies. Ideally, the "types" would not be unique devices, but the same basic two solid-state devices with different software programming. There would be multiple versions of both the basic SSCMs and the SSIMs to allow for devices of different capacities.

There are several advantages of utilizing a zonal DC power distribution system with dispersed solid-state power converters. Some of the more noteworthy advantages are cost savings associated with the elimination of large electromechanical switchgear,

improved fuel efficiency based on optimization of generator-prime mover loading, optimization of the power generation equipment to provide only the main DC power busses, minimization of power conversion steps between generator and end user, and the potential advantage of fast semiconductor devices improving shipboard power management under normal and casualty conditions. Additionally, the potential for commonality and modularity of the major components within the DC ZEDS concept adds to its appeal from a fleet logistical and training standpoint. The Navy could save appreciably in the reduced training and manning requirements as the electrical power distribution systems across the classes of ships become more common. Furthermore by standardizing equipment, lower numbers of end items are required to be maintained in the Navy supply system. In addition, as future technologies develop, the best power conversion modules available can be easily implemented into the system by application of a set of standard interface criteria.

One such technology discussed by Doerry is the Power Electronic Building Block [3].

> The Power Electronic Building Block (PEBB) is a new device that integrates within a single unit, all the elements required for generalized power processing. It will replace many single application multi-component power control circuits with a single device that delivers digitally synthesized power under device level control. PEBBs are a standard set of snap together parts that start at the semiconductor chip level and build up to the system level while integrating intelligence at various levels for custom performance - a power electronic analogy of a microprocessor.

Clearly this is an exciting possibility for the future of power electronics; however, the volume of basic research and iterative design that must be accomplished before such a device can be realized is mountainous.

The Power Electronic Building Block Testbed, or PEBB Testbed, is a test device specifically designed for research on DC-ZEDS topics. It is a full function, laboratory scale model of a single DC distribution zone. A detailed description of this test device is presented in Chapter II.

II. POWER ELECTRONIC BUILDING BLOCK TESTBED

A. PURPOSE

The purpose of the Power Electronic Building Block Testbed (PEBB Testbed) is to provide a laboratory scale test device to mimic a DC-ZEDS distribution architecture. In order to provide flexibility to perform a wide range of experiments, the PEBB Testbed includes a switching grid, DC-DC converters, DC-AC inverters and resistive/inductive links (RL Links).

B. DESCRIPTION

1. General

The testbed is based on a modified 19 inch standard instrument cabinet. The testbed is approximately 87 inches tall, has a footprint of 37 inches by 48 inches and weighs approximately 500 pounds when all devices are installed.

2. Major Components

The testbed consists of nine integral components or subsystems and all the wiring and interconnection devices. The major components include the cabinet, the switching grid, the source-side buck choppers, the load-side buck choppers, the ARCP inverters, the RL links, the three-phase input rectifier, auxiliary power supplies, and the safety circuitry. The following sections provide details on each.

a. Cabinet

The 19 inch cabinet was modified in several ways. Plexiglas sheets were placed on the sides of the cabinet to increase the usable area of the testbed. Additionally to provide mobility and stability to the device, the cabinet was placed on a wheeled carriage assembly. A fan unit was also incorporated into the cabinet to provide forced-air ventilation. Figure (2-1) is a schematic frontal view of the testbed. Subsequent sections will include a more complete description of the layout of the testbed and the individual devices incorporated in the testbed.

b. Switching Grid

A central feature of the PEBB Testbed is a switching grid that will allow for easy reconfiguration of the devices installed for testing. Figure (2-2) is a schematic of the switching grid layout. The switching grid consists of four primary DC busses (labeled BUS A - D, 50 A capacity), four auxiliary DC busses (labeled AUX BUS A - D , 60 A capacity), six device service busses (vertical busses leading to TERMINAL BLOCK 1-6, 30 A capacity), a three-phase bridge rectifier (an upgrade to a controlled rectifier as made availiable), two source-side buck converters (DC-DC1 & DC-DC2), two load-side buck converters (DC-DC3 & DC-DC4), four ARCP DC-AC inverters (ARCP1-ARCP4), four adjustable RL links (RL LINK 1 - RL LINK 4), two DC-DC contactors (S1 & S2), and two external connection terminals (TERMINAL BLOCK 7 & TERMINAL BLOCK 8). These components are connected by a network of 51 magnetically latched contactors and wiring that tie the busses together in the desired configuration.

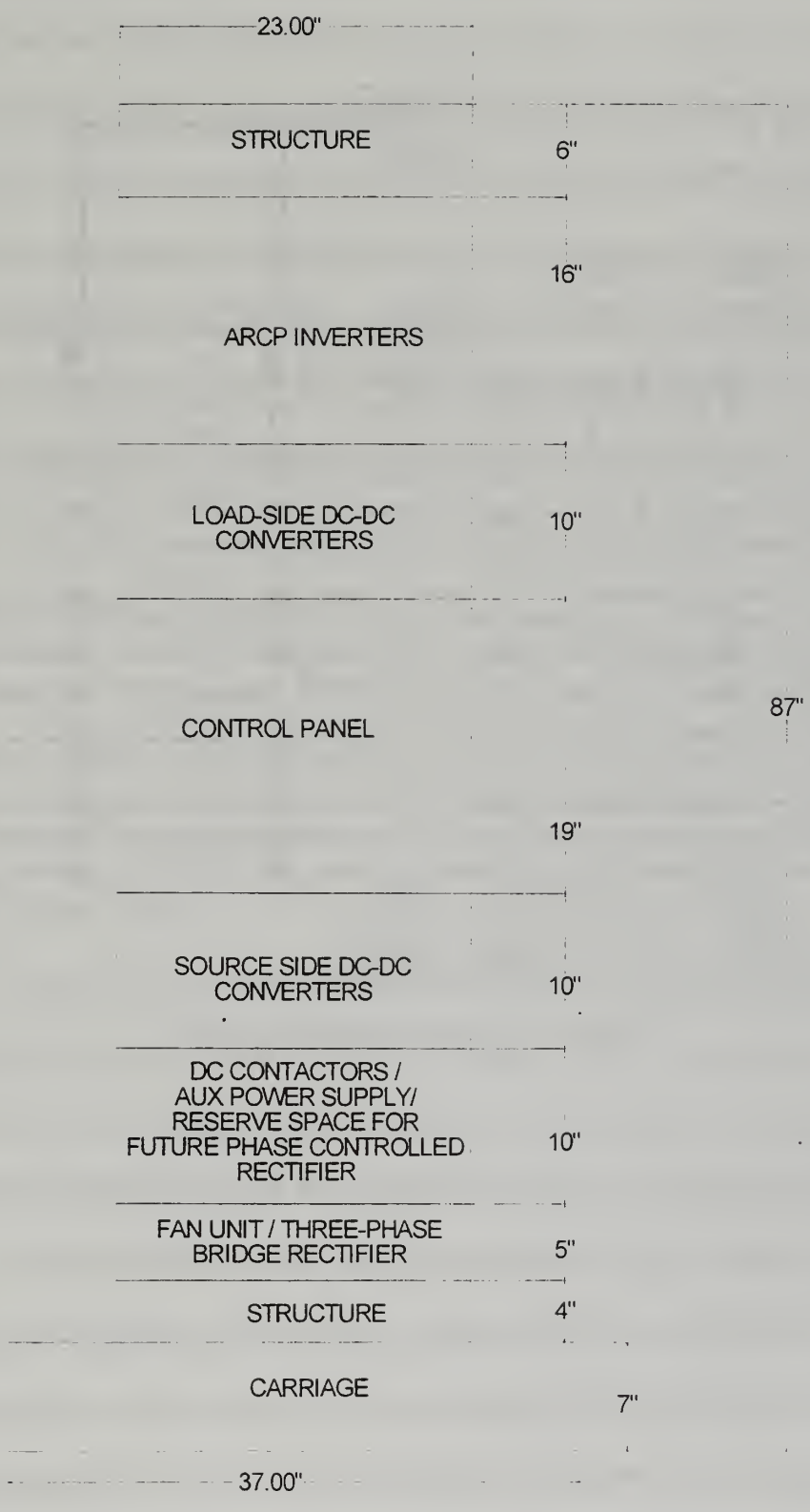

Figure 2-1, Schematic Frontal View of Testbed

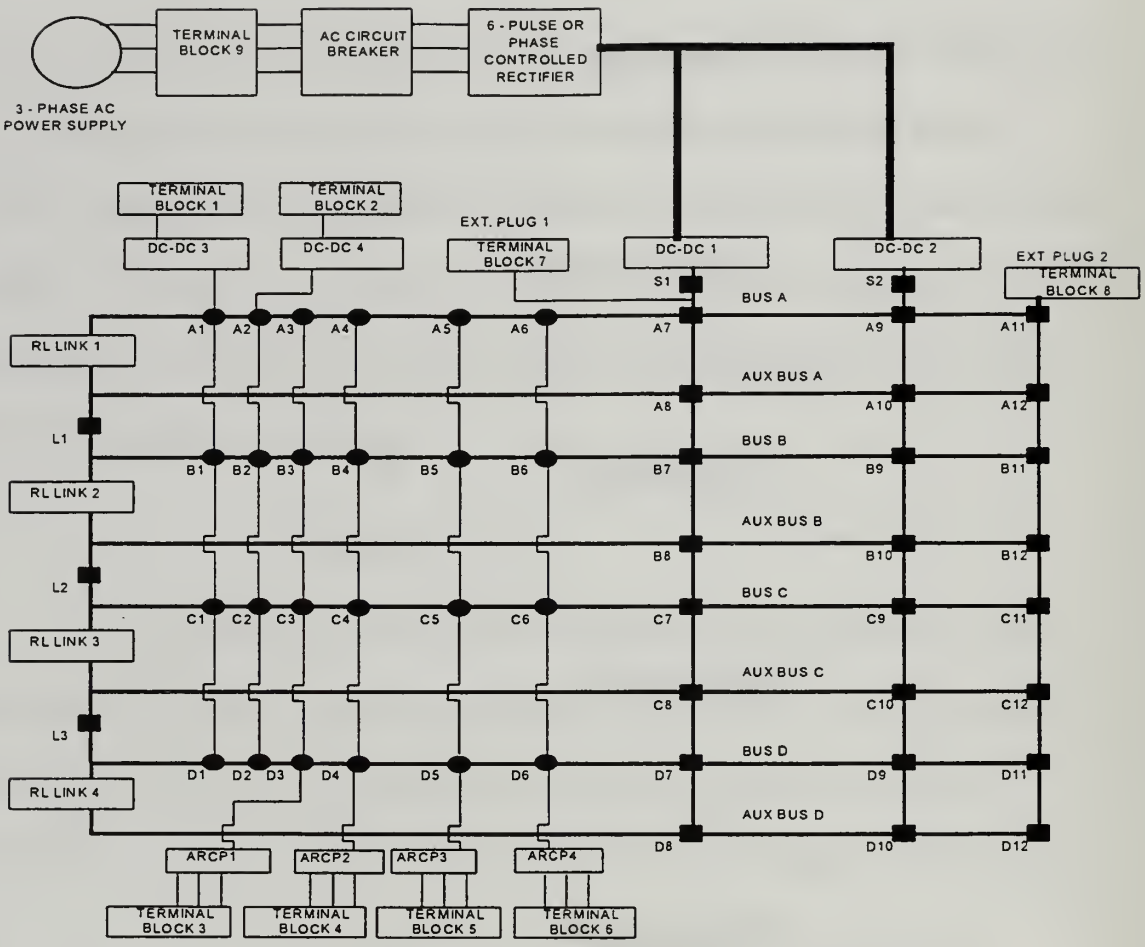

Figure 2-2, Switching Grid Schematic

This grid layout was chosen in order to provide the greatest flexibility while maintaining a simple, straight-forward architecture with a minimum number of contactors. This layout provides the operator with the ability to interconnect multiple internal devices and insert variable impedances between these devices. Additionally the external terminal blocks allow daisy-chaining of internal devices and the expansion of the testbed to incorporate new test devices.

The switching grid was built using Westinghouse AC lighting contactors which are mounted on the Plexiglas sheet on the side of the cabinet. The entire grid is wired for differential voltage; therefore, there is a "high" and a "low" wire for each bus. This allows the test cabinet to be completely isolated from the high voltage DC system. The differential wiring schematic is illustrated in Figure (2-3). In Figure (2-2), the two-pole contactors are designated by solid circles while four-pole contactors are designated by solid squares. Two-pole contactors, Westinghouse #202S1BAM, were used to connect the test devices to the main power busses (A1-6, B1-6, C1-6, D1-6). When closed, these contactors tie the device service busses to the main power busses. This provided a 30 amp capacity service to each of the test devices. The remaining switch locations used four-pole contactors, Westinghouse #202S1DAM. The contactor is wired with two sets of two poles to provide a two-pole, 60 amp capacity switch, as illustrated in Figure (2-3). These connect the 60 amp capacity busses to the source-side buck choppers, RL links and the external terminal blocks.

The current carrying capacity of the main and auxiliary busses and contactors (60 amps) was selected based on the maximum power ratings of the source-side buck choppers with a generous design margin for safety and future upgrades. Likewise, the capacity of the device service busses was based on the power ratings of the load-side buck choppers and the ARCP inverters, allowing for suitable margins. Commonality of contactors and wiring was also a design issue in the construction of the switching grid. The dual nature of the current carrying capacity also generated a need to ensure that a 60 amp current would not be drawn through a 30 amp service bus. This could happen if the configuration of the grid allowed for multiple devices to be powered by a single device

service bus. Generally speaking, the testbed as presently constructed should not be operated with more than one contactor on any given device service bus closed. The safety circuitry discussed later in this section will explain how this is prevented.

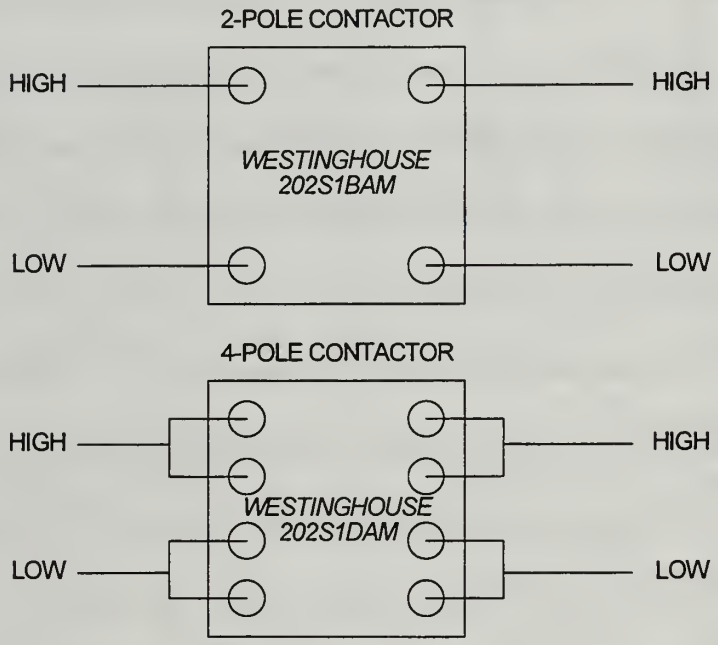

Figure 2-3, Differential Wiring Schematic

Additionally, there are two DC contactors (S1 & S2, depicted by cross-hatched squares) incorporated into the switching grid. These devices are high-voltage (600 volt), high-current (50 amp) switches that can be safely opened and closed under load, unlike the AC lighting contactors. This allows for an on-command circuit interruption capability. The contactors close when power is supplied to the source-side buck choppers from the bridge rectifier through a tap circuit that includes a mechanical switch. Figure (2-4) is a wiring schematic for the DC contactors. When the power supply to the source-side converters is interrupted, either by a fault or by actuating the mechanical switch,

switch "A", the contactors break the connection between the source-side buck shoppers and the grid. In essence a "kill switch" that separates the source-side DC-DC converters from the grid. It was found by experimentation that the DC contactors closed when approximately 60 volts are placed across the coils and opened when the voltage dropped below 40 volts. The operation of the relay associated with the safety circuitry will be described in a later section.

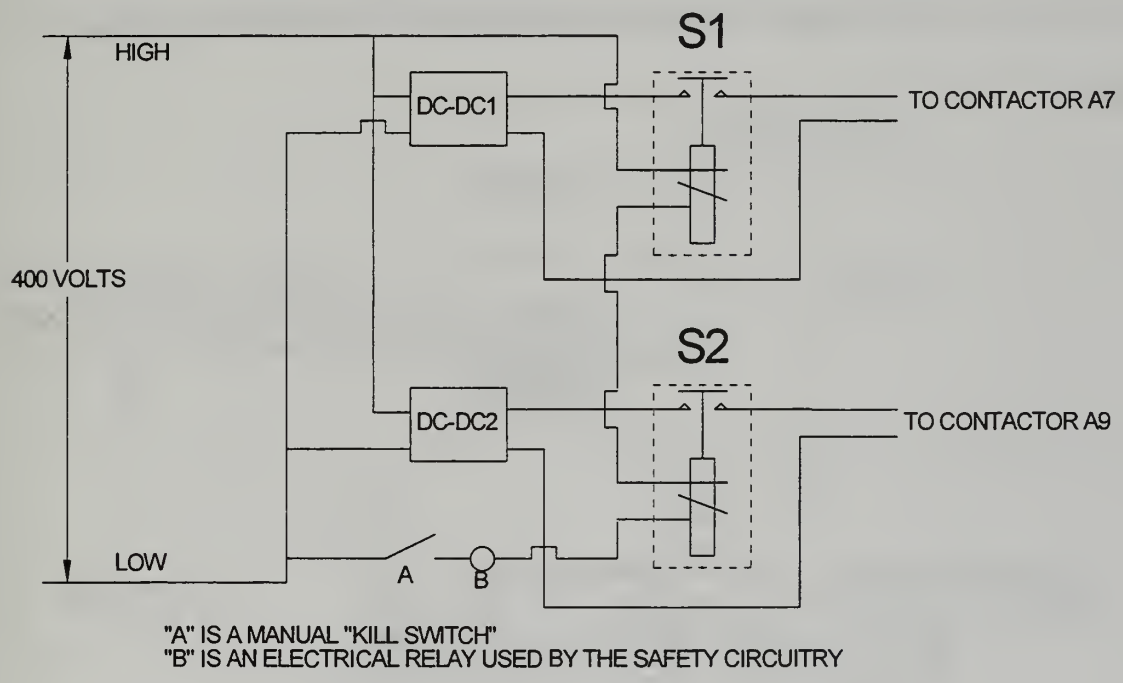

Figure 2-4, DC Contactor Wiring Schematic

The AC lighting contactors on the switching grid are controlled by a system of electrical relays actuated by toggle switches on a control panel mounted on the front of the cabinet. There are two relays used to control each AC lighting contactor: one to open the contactor and another to close the contactor. The relays use 5 V_{DC} power to control 120 V_{AC} power for the switching coils on the contactors. The state of the AC contactors

can be monitored in two ways. On the control panel, there is a red and a green LED associated with each contactor. An illuminated red LED indicates that the contactor is open, and a green LED indicates that the contactor is closed. A second method for monitoring the state of the contactors is by physical inspection. Figure (2-5) is a block diagram for the AC lighting contactor control and the LED indicator circuits. The 120 V_{AC} power is supplied be a power strip connected to a wall outlet. The 5 V_{DC} is supplied by an auxiliary power supply located inside the testbed that is discussed later in this section.

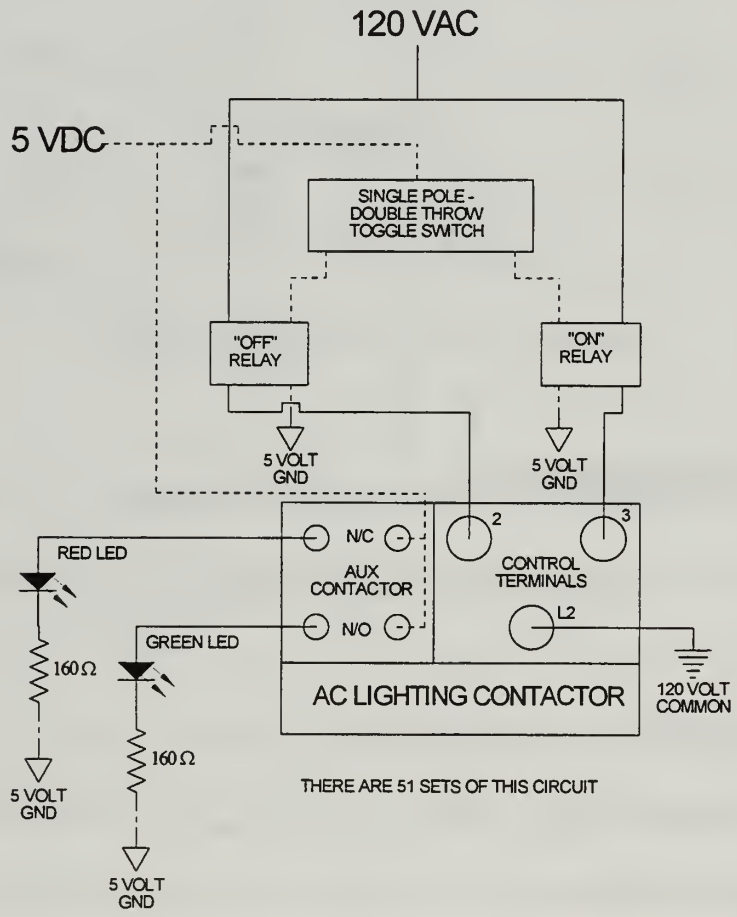

Figure 2-5, AC Lighting Contactor Control Relay and LED Indicator Circuits Block Diagram

As stated earlier, the switching grid facilitates rapid, easy reconfiguration of a DC power distribution network. Figures (2-6) and (2-7) show example configurations of the switching grid. In Figure (2-6), a simple series connection is demonstrated. In this case, a source-side buck chopper, DC-DC1, is connected to supply power to a three-phase inverter, ARCP2. Figure (2-7) show a slightly more complex topology. In this example, the source-side buck converters are configured to provide power while operating in parallel to both an inverter, ARCP1, and a load-side buck chopper, DC-DC3.

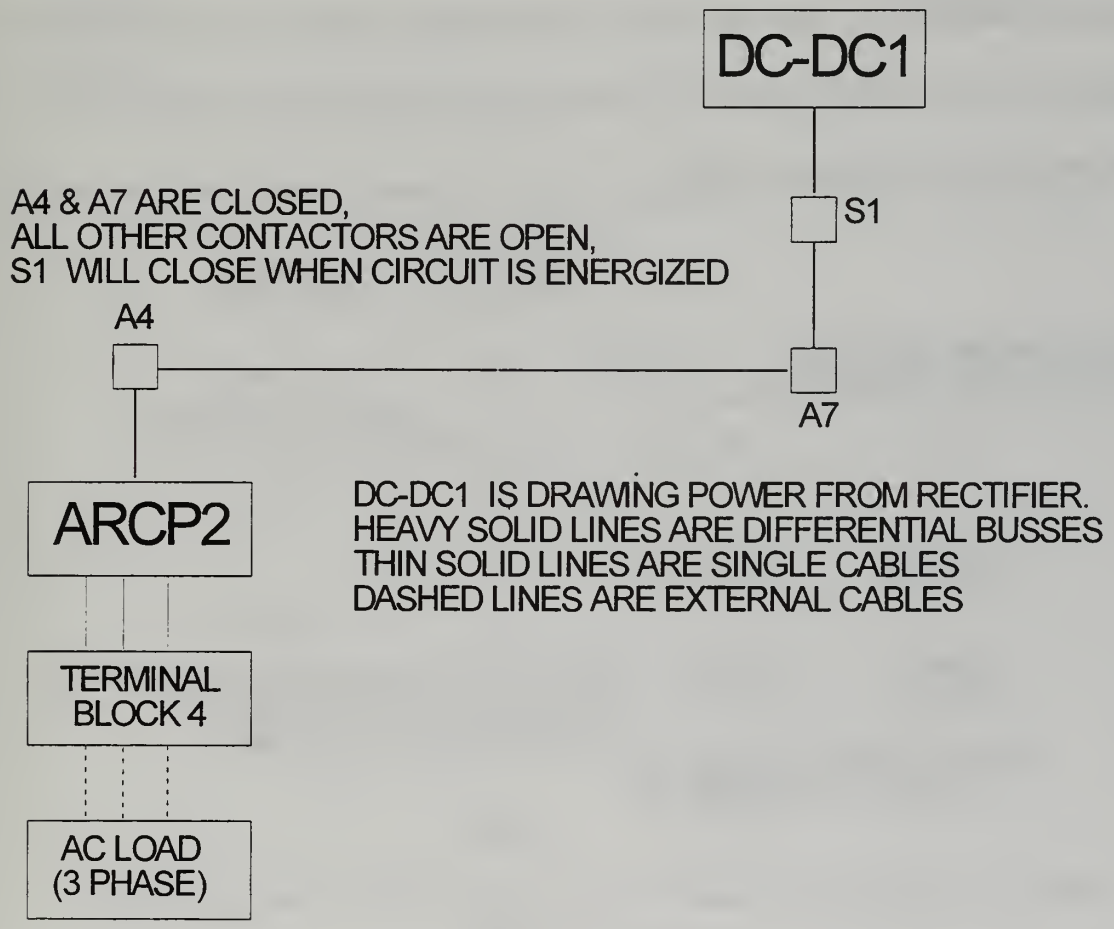

Figure 2-6, Configuration Example - DC-DC1 Supplying ARCP2

There are two external ports into the switching grid, TERMINAL BLOCK 7 & TERMINAL BLOCK 8 (Figure (2-2)). These ports allow for an external source of DC power to be supplied to the cabinet, the cabinet to power an external load or device, or for chaining together more than two devices. Figures (2-8) and (2-9) illustrate potential applications of the external ports. Figure (2-8) shows the testbed configured to provide power to a load-side buck chopper, DC-DC4, and an external load from a single source-side buck converter, DC-DC1. In Figure (2-9), an example of the flexibility of the testbed is demonstrated. Three devices are "daisy-chained" together. A source-side buck chopper, DC-DC1, provides power to a load-side buck chopper,DC-DC4, which in turn provides power to an inverter, ARCP3.

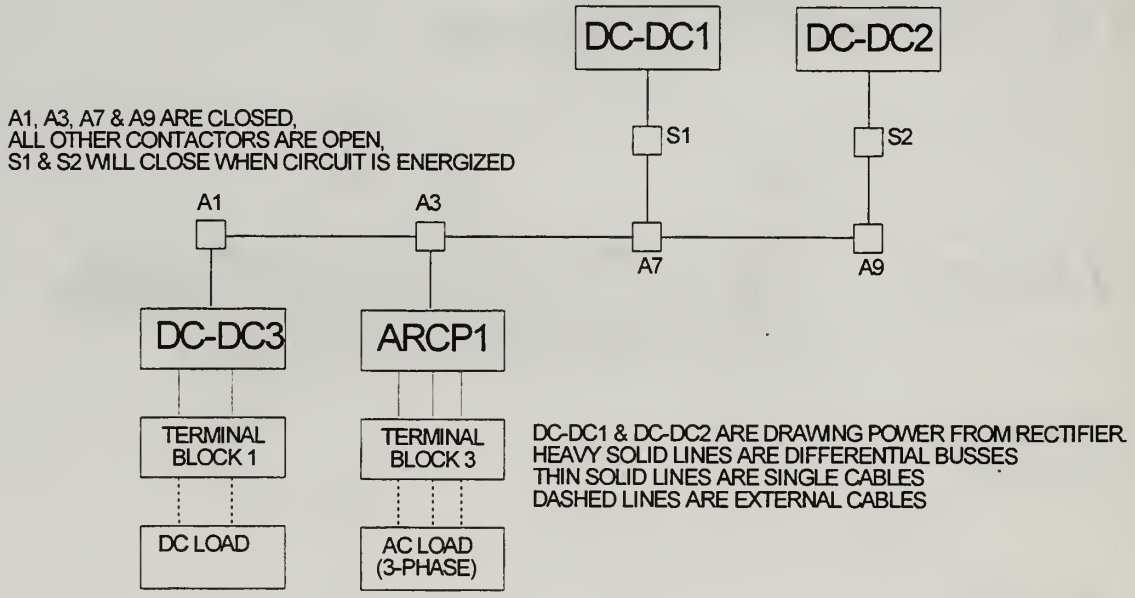

Figure 2-7, Configuration Example - DC-DC1 & DC-DC2 in Parallel Supplying ARCP1 & DC-DC3

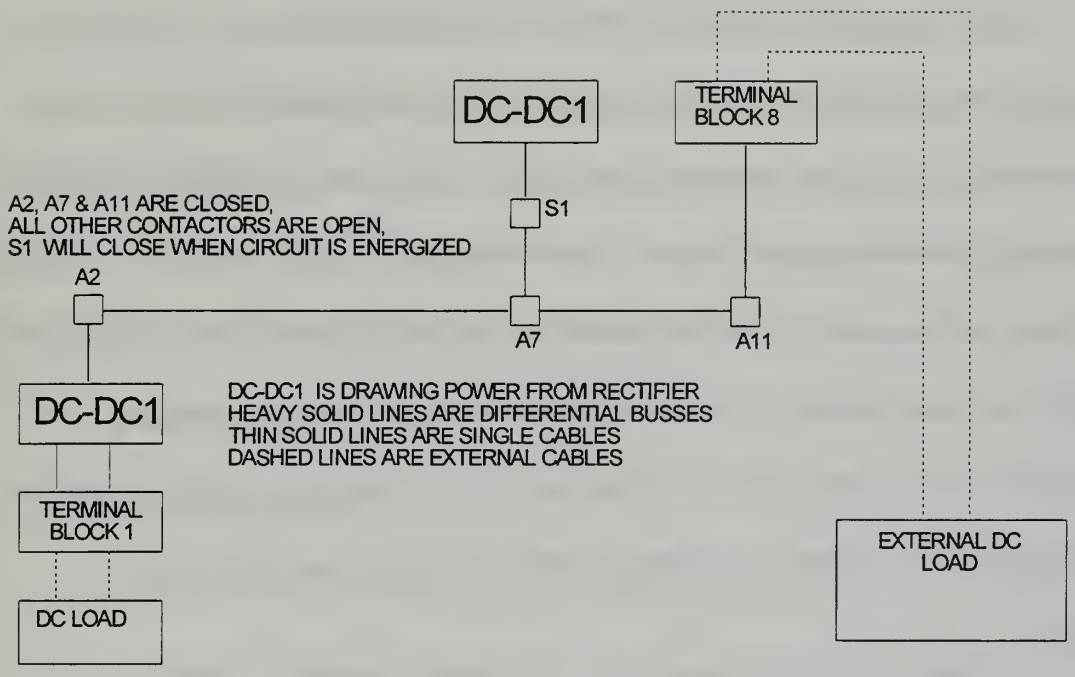

Figure 2-8, Configuration Example - DC-DC1 Supplying DC-DC4 & External Load

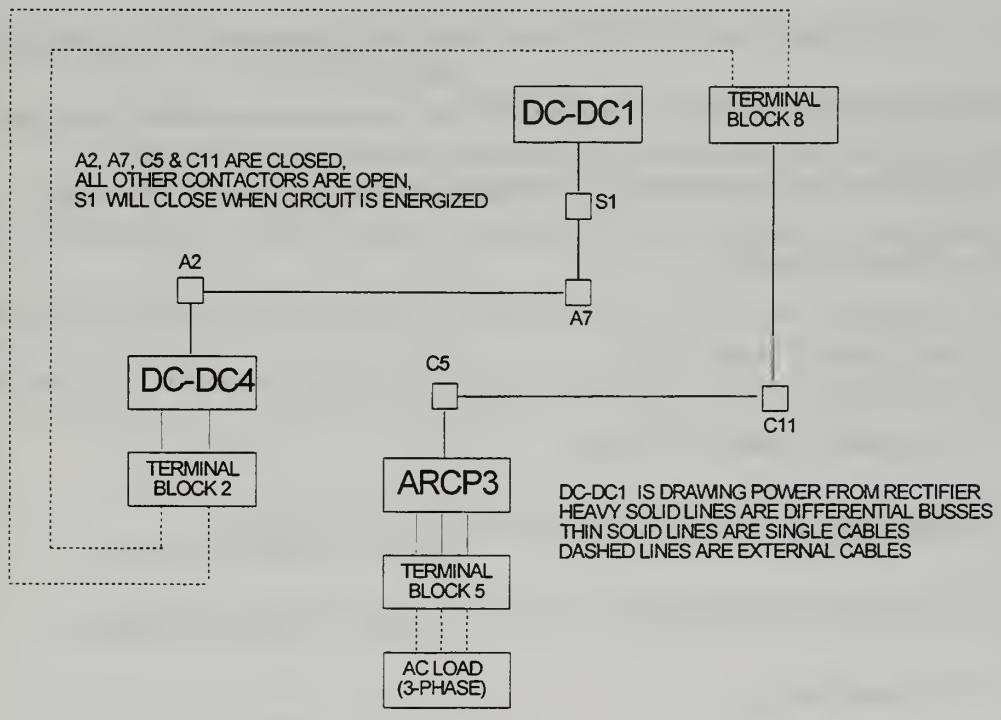

Figure 2-9, Configuration Example - DC-DC1 Supplying DC-DC4 Supplying ARCP3

The test configuration shown in Figure (2-8) would be set into the switching grid in the following manner. With the three-phase power to the rectifier off, the user would wire the external load into TERMINAL BLOCK 8. Then, he would place all contactors in the open condition and inspect them. The user would then close contactors A2, A7 and A11 (order not important). Again the user would inspect the control panel, and possibly even the contactors themselves to confirm the topology is correctly programmed. The interaction with the safety circuitry is described later in this section. Additional specific examples will be considered in Chapter IV when the experimental procedures are described.

c. Source-Side Buck Choppers (SSCM type 1)

The source-side DC-to-DC converters supply regulated 300 V_{DC} for use on the PEBB DC distribution system. The source for the converters is rectified three-phase, power. Listed below are the operating characteristics for the source-side DC-to-DC converters as listed in Allen[4]:

- Rated output power: 9 kW
- Switching frequency: ≈ 20 kHz
- Input / Output: 400V (23 A) input / 300 V (30 A) output
- Continuous operation between 10% (100 Ω) and 100% (10 Ω)loading.
- Forced-air cooling

A more detailed description of the source-side buck choppers is found in Chapter III.

d. Load-Side Buck Choppers (SSCM type 2)

The load-side DC-to-DC converters supply regulated 208 V_{DC} for use on the PEBB DC distribution system. The source for the converters is 300 V_{DC} from either the source-side DC-to-DC converters or an external source. The design characteristics for the load-side DC-to-DC converters are as described in Badorf [5]:

- Rated output power: 3 kW
- Switching frequency: ≈ 20 kHz
- Input / Output: 300V (10.4 A) input / 208 V (15 A) output
- Continuous operation between 10%(144 Ω) and 100% (14 Ω) loading.

A more detailed description of the load-side buck choppers is also found in Chapter III.

e. ARCPs (SSIM)

The Auxiliary Resonant Commutated Pole inverter (ARCP) serves as the DC-AC converter in the PEBB Testbed. The ARCP delivers regulated, three-phase AC voltage given either a regulated input DC voltage from the DC-to-DC converters or an external source. The operational characteristics of the ARCP are as described in Mayer [6].

- Peak Load Current: 25 Amps
- Resonant frequency: 250 kHz
- Switching frequency: 40 kHz (max)
- Input / Output: 300V_{DC} in (20 Amps) / 0-200 V_{AC} out at varying frequencies

Although the ARCPs are not studied in this research endeavor, they are included here for completeness in the description of the PEBB Testbed. A detailed study of the ARCP can be found in Oberley [7].

f. RL Links

The RL links are incorporated into the design to simulate the non-linear effects introduced by the physical wire runs inside of an electrical zone. Approximate dimensions of DC electric zones described by Rumburg[1] and Doerry[3] vary with the proposed type of ship; therefore, the values of the RL links considered had to also vary. The PEBB Testbed uses a multi-tap system to allow each RL link to have three distinct values of resistance/ inductance for both the "high" and the "low" cable for each main bus. The RL links are constructed of insulated #8 AWG wire, 50 amp rated capacity, wound around a 1.5 inch hollow, non-metallic, tube. The RL values for this configuration are: 1.5 μH @ 6 mΩ, 3.0 μH @ 12 mΩ, and 4.5 μH @ 18 mΩ. These values were determined by direct measurement with an inductance meter and approximate shipboard runs of two conductor 00 AWG cable for 100, 200, and 300 feet. The switching grid allows the RL links to be inserted or bypassed, but the RL values must be manually changed at a terminal block with the unit de-energized.

g. Rectifier

To provide high-voltage DC power to the testbed, a three-phase, 100 amp, 1200 volt capacity rectifier is located in the bottom of cabinet, behind the fan unit. It is mounted on a heatsink and cooled primarily by natural convection. The rectifier is

supplied with 3-phase AC power from a TERMINAL BLOCK 9 via a three-phase, 30 amp, AC circuit breaker. A preplanned upgrade to the testbed is to incorporated a phase-controlled rectifier as it is made available by the Naval Surface Warfare Center (NSWC), Carderock Division.

h. Auxiliary Power Supplies

To operate control and monitoring circuits, there are two auxiliary power supplies utilized in the PEBB Testbed, a 5 V_{DC} and a 24 V_{DC} supply. The 5 V_{DC} supply is a TDK FMP5-2K, rated for two amps. This is the primary power source for the switching grid and AC lighting contactor control panel. The nominal load demand on this power supply is approximately one amp. The 24 V_{DC} supply is a *POWER-ONE* model F24-12-A, rated for 12 amps. This is the power source for the safety circuitry, discussed below, and provides service power as needed for the test devices. Typical loading on this device is approximately four amps, assuming that it is providing service power for four ARCPs as well as the safety circuitry.

i. Safety Circuitry

The PEBB Testbed also employs two safety circuits to prevent damaging the contactors in the switching grid. The first is a high-voltage sensor on the grid itself. Its purpose is to keep the contactors from opening or closing when a high voltage exists on the grid. Since the contactors are AC devices, actuating them under heavy DC load conditions could be damaging to the device as well as dangerous to the operator. If the circuit senses a voltage above a threshold of five volts on the grid it will not allow the

contactors to be switched "on" or "off". In essence, the grid is locked into a configuration when a voltage above five volts is present on the grid. This safety circuit uses a zener diode and ceramic resistor in series, positioned across each main power bus on contactors A1, B1, C1 and D1. The voltage across the zener diode is sensed and processed by an analog circuit which controls a relay that enables or disables the 120 V_{AC} power going to the AC lighting contactor control relays. An LED that indicates if the grid is enabled is located on the control panel. Figure (2-10) is a schematic representation of this circuit.

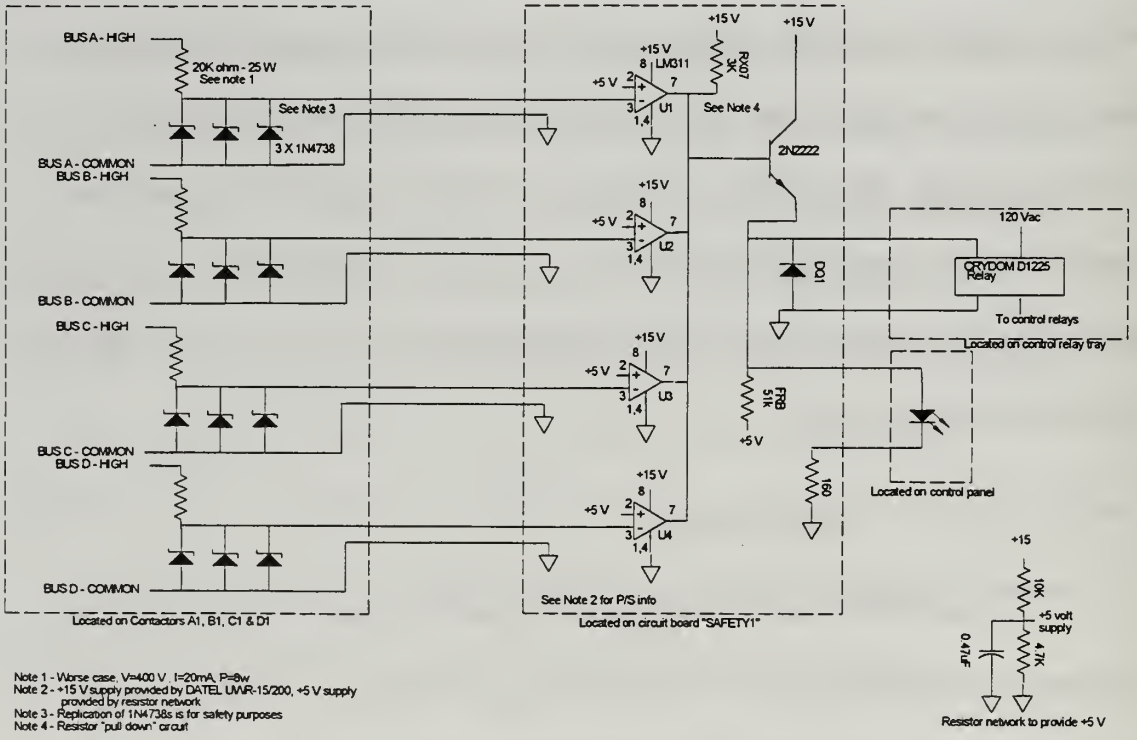

Figure 2-10, Grid High-Voltage Safety Circuit Schematic

The second safety circuit evaluates whether or not the grid is programmed in a "legal configuration". It disables the high-voltage DC input from the source-side buck

choppers if it senses a switch configuration that offers the potential to overload a contactor. The second safety circuit determines whether or not more than one contactor on a given service bus is closed at a given instant. This is to ensure that a condition will not exist where more than one load-side device is supplied by a single service bus, directly or indirectly. This could create a current draw that exceeds the capacity of the contactor. If two or more of the contactors on a service bus are closed, then the grid should not be energized. The protection circuit performs this function by sensing the state of the two-pole contactors that connect the device service busses to the main power busses and transmitting a logical "1" or "0" to a digital logic circuit. If the logic circuit senses two or more contactors on a single device service bus, it opens the circuit supplying power to the coils of the DC contactors, S1 and S2. This action keeps S1 and S2 from closing when power is applied to the source-side buck choppers. Therefore the switching grid cannot be energized. As in the first safety circuit, an LED is located on the control panel to indicate if the network configuration is "legal". Figure (2-11) is a schematic representation of this circuit.

For example, assume that DC-DC1 is going to power DC-DC3, DC-DC4, ARCP1 and ARCP2 at a high power level: Each drawing 10 amps at 300 volts. If contactors A1, A7, B1, B2, B3, and B4 were all closed and the remaining contactors were open, all 40 amps would have to pass through contactors A1 and B1 creating a potentially hazardous situation (see Figure (2-12)).

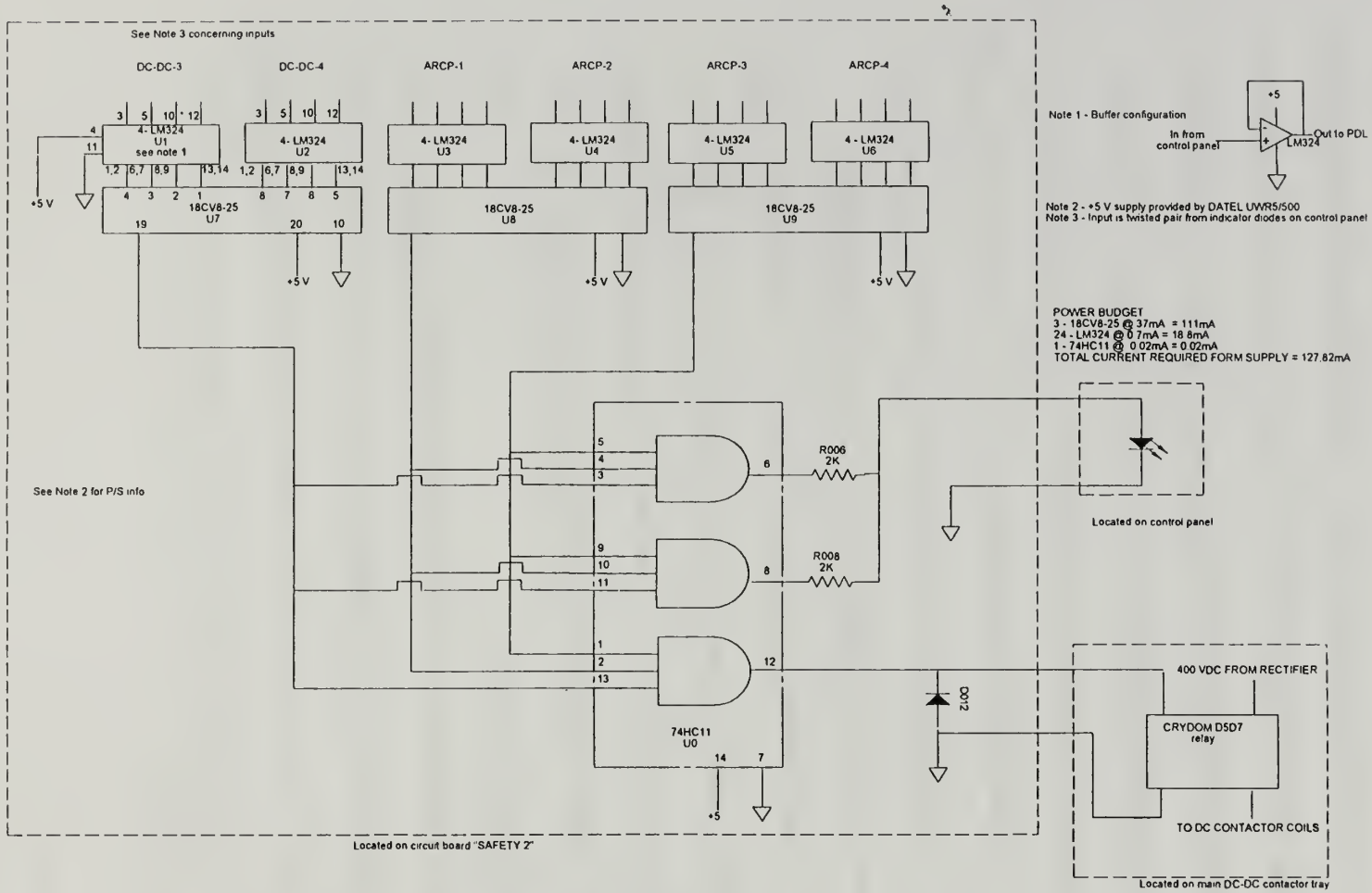

Figure 2-11, Legal Configuration Safety Circuit Schematic

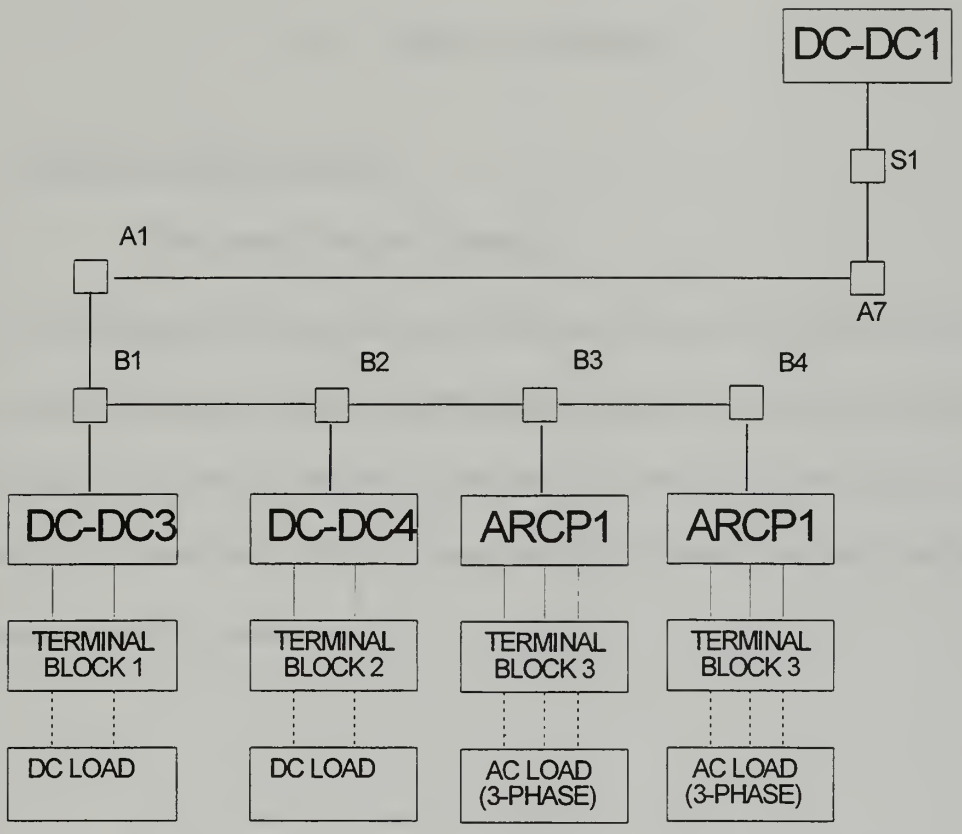

Figure 2-12, Example of an Illegal Configuration

The PEBB Testbed is a flexible test device designed specifically to support research in the field of DC ZEDS architectures. One of the central elements of the testbed, like the DC ZEDS concept, is the SSCM module. By definition, these devices must be DC-to-DC step-down converters. One of the most popular and simple topologies for this conversion process is the buck chopper. A more detailed explanation of this solid-state power conversion device is presented in Chapter III.

III. BUCK CHOPPER

A. GENERAL DESCRIPTION

1. Basic Buck Chopper Topology

The buck chopper, or step-down converter, is a DC-to-DC converter in which the input voltage is switched in a manner to produce an output voltage which is less than the input voltage. The circuit incorporates a semiconductor switch, an output filter to reduce the ripple, and a free-wheeling diode to ensure that the inductor current has a path for flow when the switch is open.

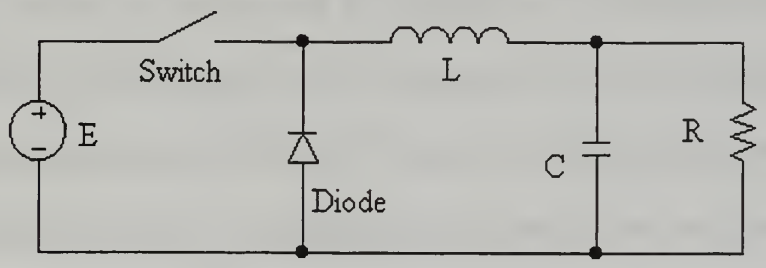

Figure 3-1, Buck Chopper Schematic

The topology for the buck chopper is shown in Figure (3-1). There are two normal modes of operation for the buck chopper depending on the current through the inductor. The primary mode of operation is characterized by the current through the inductor being continuous. In the other mode of operation the current through the inductor will reach zero and remain so until the power source supplies more power to the circuit. This thesis will only address the continuous inductor current mode of operation

due to its attractive linear input-to-output characteristic and a smaller ripple current. A description of the discontinuous inductor current operation of the circuit may be found in reference [8]. The switch and diode in the buck chopper circuit are assumed to be ideal for the derivations which follow.

Referring to Figure (3-1), the DC power source voltage is E and the switch is operated at a constant frequency. When the switch is 'on', the diode is reverse biased and the inductor accumulates energy from the source. When the switch 'opens', the source is removed from the circuit and the free-wheeling diode provides a path for the inductor current which supplies its stored energy to the capacitor and the load. The ratio of the 'on-time' to the switching period is termed the duty cycle. The capacitor reduces the output ripple to an acceptable value, determined by the sensitivity of the load. In most cases, the AC ripple is much smaller than the DC output voltage, with a reasonable value being 0.5 % or less. The net result is that the LC low-pass filter passes the average of the chopped input voltage while eliminating the high-frequency switching harmonics. For notation purposes, capital letters will denote average values while lowercase letters will denote instantaneous quantities. During the time that the switch is closed, the governing equations are:

$$E = v_L(t) + v_C(t) \tag{3-1}$$

$$E = L\frac{di_L(t)}{dt} + V_C \tag{3-2}$$

$$\frac{di_L(t)}{dt} = \frac{E - V_C}{L} \tag{3-3}$$

$$di_L(t) = \frac{E - V_C}{L} \cdot dt \tag{3-4}$$

and in the steady state:

$$I_{max} - I_{min} = \frac{E - V_C}{L} \cdot DT \tag{3-5}$$

where the value of the output capacitance is assumed to be large enough so that v_C is equal to V_C, the duty cycle of the switch is D, and the period of the switch is T. The assumption that the capacitor voltage is a DC value can be seen from:

$$v_C(t) = \tilde{v}_C(t) + V_C \tag{3-6}$$

where $\tilde{v}_C(t)$ is the capacitor AC ripple voltage and $\tilde{v}_C(t) << V_C$.

During the time that the switch is 'open', the equations which govern the circuit operation are:

$$0 = v_L - V_C \tag{3-7}$$

$$0 = L\frac{di_L}{dt} + V_C \tag{3-8}$$

$$\frac{di_L}{dt} = \frac{-V_C}{L} \tag{3-9}$$

$$di_L = \frac{-V_C}{L} \cdot dt \tag{3-10}$$

and in the steady state:

$$I_{min} - I_{max} = \frac{-V_C}{L} \cdot (1 - D) \cdot T \tag{3-11}$$

By simultaneously solving Equations (3-5) and (3-11), the expression for the input-to-output voltages can be found:

$$V_C = D \cdot E \tag{3-12}$$

Typical steady-state waveforms for the buck chopper are shown in Figure (3-2). From the beginning of a period T until the time shown as DT, the switch is 'shut' and the current through the inductor i_L rises. The current through the switch i_s is identical to the inductor current while the switch is 'shut' so it also rises during this time interval. The diode is reverse biased so the diode current i_D is zero during this interval. The source voltage is connected to the input-side of the inductor while the capacitor is connected to the output-side of the inductor, so the inductor voltage v_L is seen as the difference between the two for this interval. When the switch 'opens', the source is isolated from the rest of the circuit and the free-wheeling diode allows for current to flow as described previously.

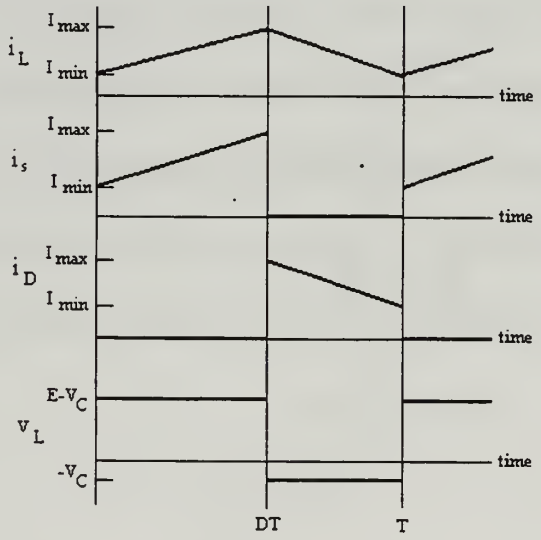

Figure 3-2, Typical Waveforms for a Buck Chopper with Continuous Inductor Current

During this interval the inductor current falls while the switch current is zero due to the switch being 'open'. The diode current is identical to the inductor current during

this interval. Finally, by applying Kirchhoff's voltage law to the loop which includes the inductor, diode and capacitor, and assuming zero voltage drop across the diode, the inductor voltage is seen to be equal to the opposite of the capacitor voltage. These waveforms should be referred to during the following discussion.

In order to select an inductor for the circuit which will prevent the discontinuous current mode from occurring and thus taking advantage of the linear input-to-output transfer relationship, the average inductor current is found:

$$I_L = \frac{I_{max} - I_{min}}{2} \tag{3-13}$$

and the average load current is found:

$$I_R = \frac{V_C}{R} = I_L \tag{3-14}$$

where the inductor current is assumed to be equal to the load current due to the large capacitor size. By setting equal Equations (3-13) and (3-14), the maximum inductor current is found:

$$\frac{I_{max} + I_{min}}{2} = \frac{V_C}{R} \tag{3-15}$$

$$I_{max} = \frac{2V_C}{R} - I_{min} \tag{3-16}$$

Substituting Equation (3-16) into Equation(3-11) yields:

$$I_{min} - \frac{2V_C}{R} + I_{min} = \frac{-V_C}{L} \cdot (1 - D) \cdot T \tag{3-17}$$

$$2I_{min} = \frac{-V_C}{L} \cdot (1 - D) \cdot T + \frac{2V_C}{R} \tag{3-18}$$

By setting the minimum inductor current to zero, the value of the critical inductance is found:

$$L_{crit} = \frac{T \cdot R}{2} \cdot (1 - D) \tag{3-19}$$

This minimum inductance value must be satisfied in order to ensure continuous current operation of the buck chopper.

2. Prefilter

To ensure that the input voltage, E, was as constant as possible, an inductor-capacitor (LC) prefilter was incorporated into the basic buck chopper design. The values of the components were selected to further reduce the ripple from the DC source, while maintaining commonality to the maximum extent possible. Figure (3-3) illustrates how the prefilter is incorporated into the basic buck chopper topology.

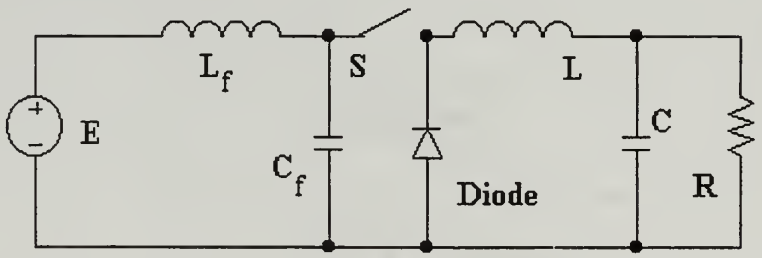

Figure 3-3, Simplified Buck Chopper Circuit with Prefilter

3. IGBT Driver Circuit

The main switch used in the construction of the power section requires a set of input voltages on the gate terminal which are properly controlled in magnitude with a

relatively high value of source and sink currents in order to operate properly. The circuit constructed for use with the IGBT is shown in Figure (3-4).

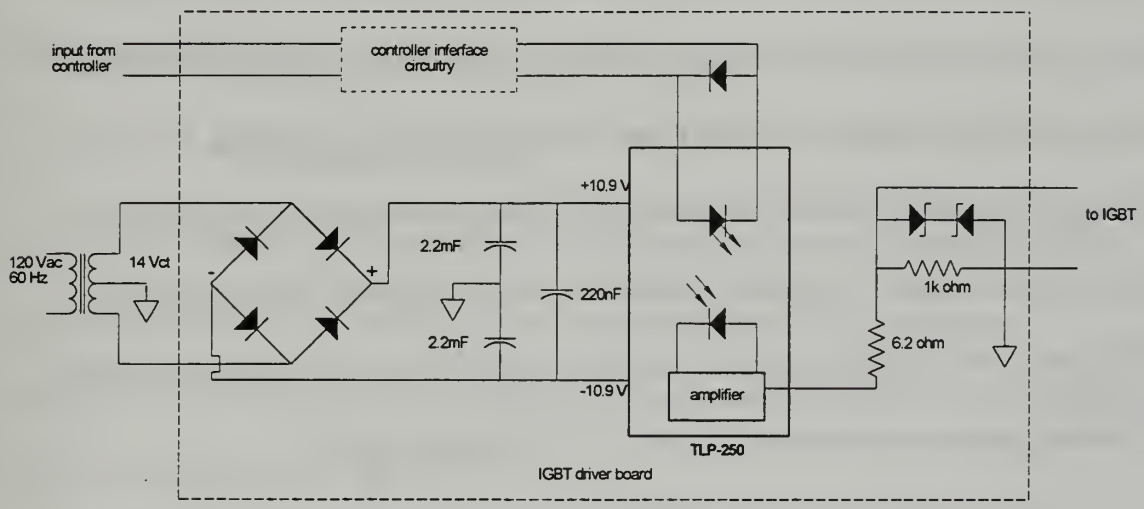

Figure 3-4, IGBT Gate Drive Circuit

The heart of the driver circuit is the TOSHIBA TLP 250 gate drive photo IC coupler. This device combines the high speed, high gate current, and optical isolation of the control circuit in one package for ease of use. The 120/14 V_{AC}, center-tap transformer, diode configuration, and 2.2 mF capacitors produce an unregulated $\pm$10.9 V_{DC} power supply referenced from a floating ground. The 220 nF capacitor reduces any high-frequency noise seen on the power supplies as a result of switching transients on the TLP 250. A high-speed diode is connected in anti-parallel to the TLP 250 light emitting diode to protect the device from excessive reverse current. The zener diode pair prevent the voltage on the IGBT gate from becoming too large thus protecting the gate circuit from damage. Finally, the output resistor network ensures proper impedance matching of

the IGBT gate and driver circuit while providing current limiting to the TLP 250 output transistors.

The operation of the circuit is straightforward. A 15 V input to the driver circuit will cause the LED on the TLP 250 chip to assume the 'on' state. The optical sensor within the chip will detect the condition of the diode and cause the output amplifier on the chip to set the voltage on the IGBT gate 'high' at + 10.9 V, thus turning it 'on'. Use of the optical isolator allows the output signal to float up to the switch voltage while the input signal remains at an isolated ground. The stray capacitance, associated with the IGBT gate circuit and leads between the IGBT and driver circuit, is rapidly charged due to the high source current capability of the TLP 250 output amplifier.

When the input voltage to the driver circuit is set to -15 V, the TLP 250 diode is turned 'off', and the output amplifier will set the gate voltage to -10.9V. Once again, the current sinking ability of the output amplifier enables the charge on the IGBT gate to be removed very rapidly, enhancing the ability of the driver to be used in higher speed circuit applications.

B. SOURCE-SIDE BUCK CHOPPER (SSCM #1)

1. Operating Parameters

As discussed in Chapter II, an input voltage of 400 V_{DC} and an output voltage of 300 V_{DC} were selected for the laboratory scale implementation of the PEBB Testbed. Based on Equation(3-12), this resulted in a nominal duty cycle of 0.75. The operating frequency for the switch was selected to be approximately 20 kHz as a compromise

between audible noise, switch power loss and filter component size. Switch power loss increases linearly with frequency while component sizes decrease. The resulting period of the switch is 50 μsec. A full power rating was determined to be 9 kW, a value large enough to demonstrate the PEBB concept but small enough to allow for laboratory construction and testing.

2. Component Selection

A 10% load of 100 Ω was selected for determining a critical inductance of 737 μH (see Equation (3-17)). In order to have a load-side filter with a low resonant frequency, a 400 μF capacitor was selected. The components utilized in constructing the circuit are summarized in Table (3-1).

Switch	International Rectifier IRGT1090U06 Insulated Gate Bipolar-Junction Transistor (IGBT), with anti-parallel diode
Capacitor	Mallory 400 μF, 450 V_{DC}
Inductor (hand wound)	760 μH (DC-DC1) 860 μH (DC-DC2)

Table 3-1, Circuit Components

The combined switch and diode pack used in the buck chopper is a high-speed (25 to 100 kHz) and high-power (600 V, 90 A) device. As such, the voltage drop and switching loss during steady-state operation are small compared to the voltages and currents being switched, thus justifying the assumption that the voltage drops across these components are zero for the equations derived in this chapter.

3. Prefilter

The prefilter for the supply-side buck choppers was constructed with a 2000μF computer-grade electrolytic capacitor along with hand-wound inductor. Table (3-2) details the components used in the prefilter.

Capacitor	Sprague Powerlytic 2000 μF, 450 V_{DC}
Inductor (hand wound)	425 μH (DC-DC1) 433 μH (DC-DC2)

Table 3-2, Prefilter Circuit Components

4. Controller

The supply-side buck choppers employ an analog control technique designed by Dr. R. W. Ashton of the Naval Postgraduate School. Monitored parameters are sensed from the buck chopper, fed into the control circuitry and a duty cycle, D, is output to the IGBT driver circuit through a twisted wire pair. The analog control algorithm employed for the source-side buck choppers is:

$$d(t) = Dss - \left(h_v + h_n \int dt\right)\left(v_0 - v_{ref} - \frac{i_0}{10}\right) - h_i\left(i_L - i_0\right) \qquad (3\text{-}20)$$

where,

$d(t)$ = time-varying duty cycle
Dss = steady-state duty cycle
h_v = voltage gain
h_n = integrator gain
h_i = current gain
v_0 = output voltage
v_{ref} = reference voltage
i_0 = load current
i_L = inductor current

The controller also has circuitry to perform auxiliary functions such as limiting the current, temperature sensing and buck chopper startup. Additional information on the analog control algorithm and gain selection can be found in Badorf [5]. A complete

description of the supply-side buck chopper design, fabrication and testing can be found in Allen [4].

C. LOAD-SIDE BUCK CHOPPERS (SSCM #2)

1. Operating Parameters

As discussed in Chapter II, an input voltage of 300 V_{DC} to the load-side buck choppers and an output voltage of 208 V_{DC} were selected for the laboratory scale implementation of the PEBB Testbed. This resulted in a nominal duty cycle of 0.693 based on Equation (3-12). Again, the operating frequency for the switch was selected to be approximately 20 kHz as a compromise between audible noise, switch power loss and filter component size. The resulting period of the switch is 50 μsec. A full power rating was determined to be 3 kW, a value consistent with the scale of the PEBB Testbed.

2. Component Selection

A load resistance of 150 Ω was selected in order to define the minimum load current expected, yielding a critical inductance, from Equation (3-19), of 1.15 mH. The components utilized in constructing the circuit are summarized in Table (3-3).

Switch	International Rectifier IRGT1090U06 Insulated Gate Bipolar-Junction Transistor (IGBT), with anti-parallel diode
Capacitor	Mallory 400 μF, 450 V_{DC}
Inductor (hand wound)	1.32 mH, (DC-DC3) 1.35 mH, (DC-DC4)

Table 3-3, Circuit Components

As in the case of the supply-side buck chopper, the combined switch and diode pack used is a high-speed (25 to 100 kHz) and high-power (600 V, 90 A) device so that the voltage drops across the IGBT and the anti-parallel diode are negligible.

3. Prefilter

The prefilter for the load-side buck choppers was constructed in a similar manner as the supply-side buck chopper: a 400μF computer-grade electrolytic capacitor and a hand-wound inductor. Table (3-4) details the components used in the prefilter.

Capacitor	460 μF (2 Sprague Powerlytic 230 μF, 450 V_{DC})
Inductor (hand wound)	422 μH (DC-DC3) 437 μH (DC-DC4)

Table 3-4, Prefilter Circuit Components

4. Controller

The load-side buck choppers were controlled by a digital signal processing (DSP) control unit (The PEBB Universal Controller) developed by Mr. T. Duong of the Naval Surface Warfare Center (Code 813), using an algorithm derived from Equation (3-20). The modified control algorithm as reported in Hanson [9] is:

$$\begin{aligned} d[n+1] = Dss[n] - h_v\left(v_{out}[n] - V_{ref}\right) - \frac{h_n T}{2}\left(v_d[n-1] + v_d[n]\right) \\ - v_{dint}[n-1] - h_i\left(i_L[n] - i_{out}[n]\right) \end{aligned} \tag{3-21}$$

Again, inputs are sensed, then fed into the control circuitry and a duty cycle, D, is output to the IGBT driver circuit through an optical link. The DSP control of the load-

side buck choppers facilitates rapidly tuning the control gains, modifying the control algorithm and adjusting the control bandwidth.

The focus of this research effort is to study the effects of networking buck choppers. This will be accomplished by using the PEBB Testbed to interconnect two source-side buck choppers (SSCM #1)and two load-side buck choppers (SSCM #2). The following chapter describes the experiments conducted to support this undertaking.

IV. EXPERIMENTAL PROCEDURE

A. OVERVIEW

This research is geared toward investigating issues relating to the interconnections and topologies associated with a DC ZEDS architecture. The phenomena studied in this research endeavor is the macroscopic transient response associated with changes in the converter loading characteristics and line inductance levels of the network. Settling time, overshoot and the presence of oscillations are the subjects of primary interest. These characteristics will be observed and analyzed with the aid of standard test equipment and oscilloscopes.

B. GENERAL PROCEDURE

The general experimental procedure consists of three tests on four different configurations of networked buck choppers. The buck choppers are operated at a variety of load conditions and are interconnected using the various inductance links available in the PEBB Testbed. The configurations examined are a simple series connection between a single source-side buck chopper and a single load-side buck chopper, a single source-side buck chopper in series with two load-side buck choppers, two source-side buck choppers connected in parallel, tied in series to a single load-side buck chopper, and two source-side buck choppers connected in parallel, tied in series to two load-side buck choppers. Detailed topologies used for each testing configuration are presented later in this chapter. The three basic tests considered are a step increase in the load (a step change in the load resistance) on the load-side buck chopper, a step decrease in the load

load (a step change in the load resistance) on the load-side buck chopper, and a cycled periodic change in the load demand on the load-side buck chopper. In order to assimilate a catalog of data for making stability and performance conclusions, each of the three load tests described above was conducted for each configuration at five levels of line inductance between the source-side buck chopper and the load-side buck chopper. Also, each of the three basic tests was conducted at two levels of source-side buck chopper loading, a light and a heavy load condition for each line inductance level.

1. Loading of Load-Side Buck Chopper

The first basic test was structured to examine a step increase in the load demand on the load-side buck chopper. The steady-state load was increased from 10% (300 watts - 1.5 amps @ 200 volts) of rated capacity to 90% (2.7 kilowatts - 13.5 amps @ 200 volts) of rated capacity. The second basic test was structured to examine a step decrease in the load on the load-side buck chopper from 90% of rated capacity to 10% of rated capacity. The final basic test was a periodically changing load demand. The load-side buck chopper load was switched between 10% of capacity for 0.01 seconds and 90% of capacity for 0.01 seconds, a 50 Hz cycling frequency. This frequency was chosen arbitrarily; it was convenient to implement with the equipment available and allowed for the acquisition of meaningful data.

The step changes in output power were implemented using a load bank configuration as shown in Figure (4-1). The loadbanks and transistors used in these experiments were standard *INVERPOWER,* laboratory experimental modules. The loadbanks were model P108-RLs, rated for 3 kW at either 115 Volts or 230 Volts

depending on the internal configuration. Single transistors on a model P111-VSI module were used for the switching action. These devices are rated for 100 A and 450 Volts. Additional *INVERPOWER* modules were used as required for providing logic power, signal amplification and voltage isolation.

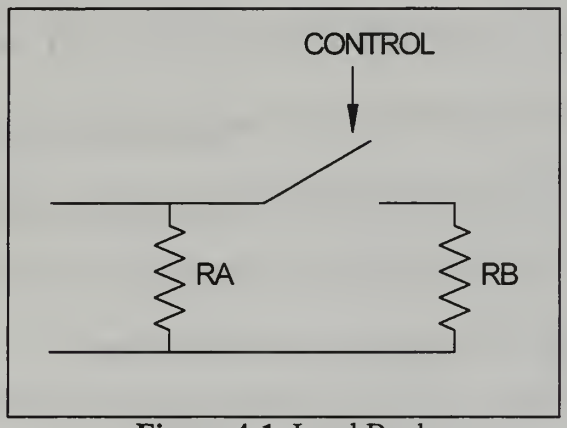

Figure 4-1, Load Bank

A full load to light load condition was executed in the following manner: The network was energized with control power applied to the power transistor, the system was allowed to come to steady state, the control power was cut, removing the second resistor, R_B, from the network. Similarly, a light load to full load test was realized by energizing the network without control power applied to the power transistor. The system was allowed to come to steady state. Then the control power was activated, placing the second resistor, R_B, in the network. A full load to light load to full load periodic variation was performed by using a signal generator to provide a square wave input to the power transistor. The square wave was set to 50 Hz with a 50% duty cycle. The system was allowed to come to steady state as in the light load to full load test (no control applied). To begin the test, the square wave was applied as the control.

2. Line Inductance

Levels of line inductance used in the experimentation were selected to give a wide range of data centered on the values of line inductance derived from the general design parameters described by Rumburg[1] and Doerry[3]. Using the RL-links on the testbed, approximate line inductance of 0.0 μH, 4.5 μH, 9.0 μH, 13.5 μH, and 18.0μH were inserted between the supply-side and load-side buck choppers. This was done by setting all four RL links to 4.5 μH and placing the RL links in series by manipulating the testbed switching grid, Figure (2-2). The actual switch configurations used will vary with the testing configuration, each will be discussed later in this chapter.

3. Loading of Source-Side Buck Chopper

Source-side buck chopper loading was performed at a light level and a heavy level. For the light load condition, an additional 1 kilowatt pure resistive load was attached to each supply-side buck chopper. This corresponds to 11% of the rated load. This load was situated in parallel with the output capacitor of the supply-side buck chopper, before the RL links and the load-side buck chopper(s). An external terminal block (TERMINAL BLOCK 8) was used to insert this resistance (See Figure (2-8)). Tests were also run at a heavily loaded condition. In these cases, the source-side buck choppers had pure resistive loads, sized to bring the load up to approximately 90% of rated capacity, attached as in the light load case.

4. Monitored Parameters

As stated in the overview, the response of the network to a transient is the focus of this research. To observe the network response, the output current and voltage levels

for each tested solid-state device, as well as the voltage and current servicing the supply-side buck chopper resistive load, were monitored for all of the experiments. Additional parameters were also monitored on an "as required" basis to aid in identifying anomalies and potential subjects for future research. These parameters include but are not limited to inductor currents, IGBT driver signals, and control signals.

C. TESTING CONFIGURATIONS

The four topologies investigated in this research effort are expounded upon in the following sections.

1. One Buck Chopper Feeding One Buck Chopper

a. Topology

The basic testing topology used for this series of tests is shown in Figure (4-2). The resistance values used are as follows: $R_1 = 90\ \Omega$ (light loading), $R_1 = 18\ \Omega$ (heavy loading), $R_2 = 144\ \Omega$, $R_3 = 18\ \Omega$.

b. Line Inductance

The switching grid, Figure (2-2), was manipulated to place line inductance between a supply-side buck chopper (DC-DC1) and a load-side buck chopper (DC-DC3) in the following manner: Starting with all contactors open, to place 0.0 μH of line inductance, contactors A-1, A-7 and A-11 were closed. To increase the line inductance to 4.5 μH, contactors A-7 and A-11 were opened and contactors A-8 and A-12 were closed. A 9.0 μH line inductance was realized by placing RL-link 1 and RL-link 2 in

series: A-8 and A-12 were opened and contactors B-8, B-12 and L-1 were closed. In a similar manner, B-8 and B-12 were opened and C-8, C-12 and L-2 were closed to provide 13.5 μH of line inductance. Finally, C-8 and C-12 were opened and D-8, D-12 and L-3 were closed to place all four RL links in series, providing 18.0μH of line inductance.

c. Load-Side Buck Chopper Loading

The procedure used in this phase was exactly as detailed above in the general procedure section of this chapter. Table (4-1) is a tabular representation of the 30 separate experiments to be performed in this phase of the research.

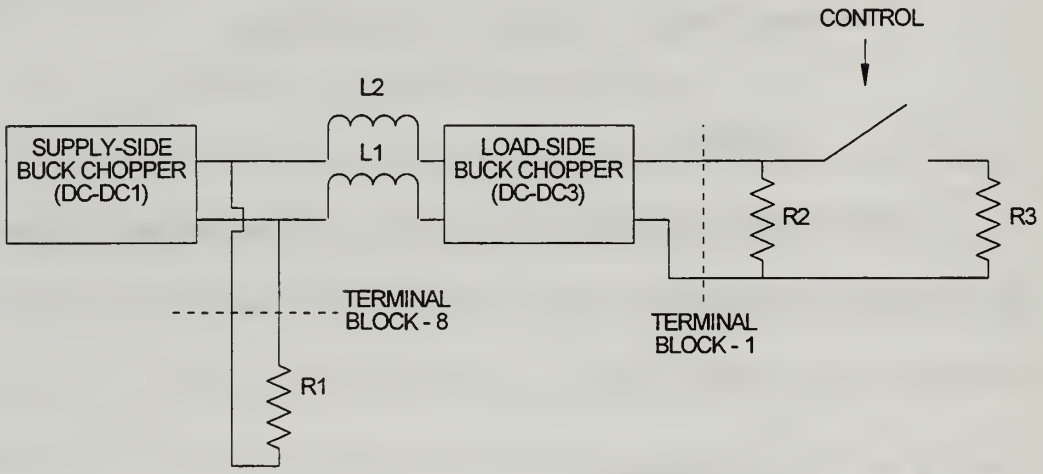

Figure 4-2, Topology Used For Series Connection Of Two Buck Chopper

	Light load on DC-DC1			Heavy load on DC-DC1		
	DC-DC3			DC-DC3		
Line Inductance (μh)	10%→ 90%	90%→ 10%	Oscillation	10%→ 90%	90%→ 10%	Oscillation
0.0	EXP A-1	EXP A-6	EXP A-11	EXP A-16	EXP A-21	EXP A-26
4.5	EXP A-2	EXP A-7	EXP A-12	EXP A-17	EXP A-22	EXP A-27
9.0	EXP A-3	EXP A-8	EXP A-13	EXP A-18	EXP A-23	EXP A-28
13.5	EXP A-4	EXP A-9	EXP A-14	EXP A-19	EXP A-24	EXP A-29
18.0	EXP A-5	EXP A-10	EXP A-15	EXP A-20	EXP A-25	EXP A-30

Table 4-1, Experimental Phase A - Series Connection Of Two Buck Choppers

2. One Buck Chopper Feeding Two Choppers in Series

a. Topology

The testing topology used for this series of tests is shown in Figure (4-3). The resistance values used are as follows: $R_1 = 90\ \Omega$ (light loading), $R_1 = 28\ \Omega$ (heavy loading), $R_2 = R_4 = 144\ \Omega$, $R_3 = R_5 = 18\ \Omega$.

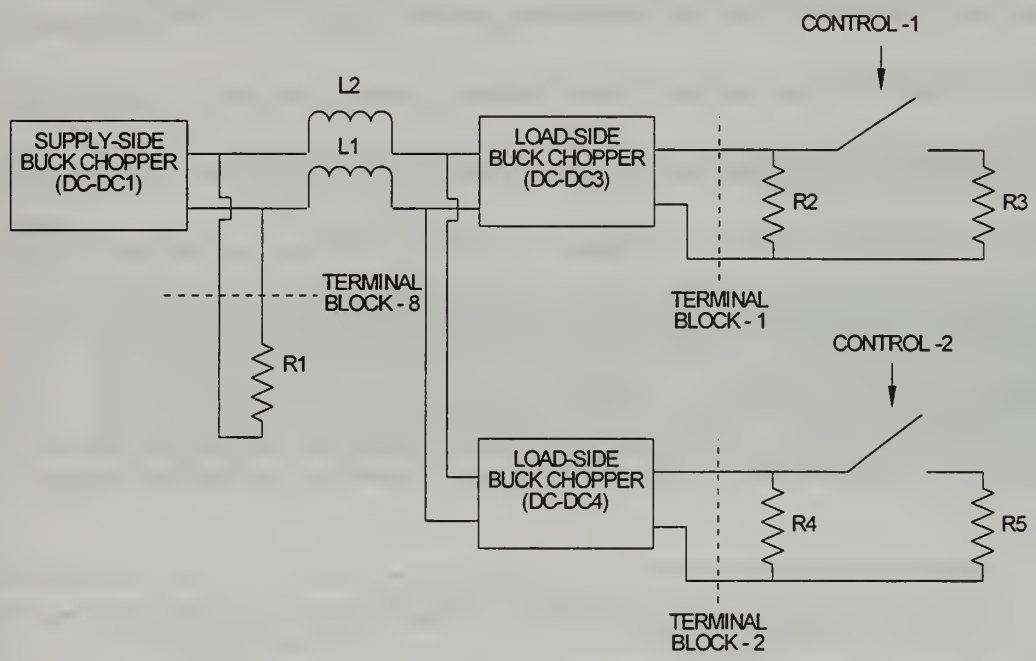

Figure 4-3, Topology Used For One Buck Chopper Feeding Two Buck Choppers

b. Line Inductance

The switching grid was manipulated to place line inductance between the supply-side buck chopper (DC-DC1) and the two load-side buck choppers (DC-DC3 & DC-DC4). The procedure used in the simple series connection was repeated with one

variation, contactor A-2 was also closed in the initial setup and remained closed throughout this phase of the testing.

c. Load-Side Buck Chopper Loading

The general procedure was slightly modified for this phase of testing. DC-DC3 was again used to investigate the system transients. The same three basic tests were performed as before, but with DC-DC4 operating at either a high or a low load demand. Tables (4-2a) and (4-2b) are tabular representations of these experiments. Additionally, a non-synchronous variable load test was performed. For this experiment, the load bank for DC-DC3 was fed the same control signal as before (50 Hz), but the load bank for DC-DC4 was fed a 75 Hz control signal. This was done at all five values of line inductance and for both supply-side buck chopper load demand conditions. Table (4-2c) encapsulates these procedures. A total of 70 experiments were conducted in this phase.

	DC-DC4 at 10% load					
	Light load on DC-DC1			Heavy load on DC-DC1		
	DC-DC3			DC-DC3		
Line Inductance (μh)	10%→ 90%	90%→ 10%	Oscillation	10%→ 90%	90%→ 10%	Oscillation
0.0	EXP B-1	EXP B-6	EXP B-11	EXP B-16	EXP B-21	EXP B-26
4.5	EXP B-2	EXP B-7	EXP B-12	EXP B-17	EXP B-22	EXP B-27
9.0	EXP B-3	EXP B-8	EXP B-13	EXP B-18	EXP B-23	EXP B-28
13.5	EXP B-4	EXP B-9	EXP B-14	EXP B-19	EXP B-24	EXP B-29
18.0	EXP B-5	EXP B-10	EXP B-15	EXP B-20	EXP B-25	EXP B-30

Table 4-2a, One Buck Chopper Feeding Two Buck Choppers

	DC-DC4 at 90% load					
	Light load on DC-DC1			Heavy load on DC-DC1		
	DC-DC3			DC-DC3		
Line Inductance (μh)	10%→ 90%	90%→ 10%	Oscillation	10%→ 90%	90%→ 10%	Oscillation
0.0	EXP B-31	EXP B-36	EXP B-41	EXP B-46	EXP B-51	EXP B-56
4.5	EXP B-32	EXP B-37	EXP B-42	EXP B-47	EXP B-52	EXP B-57
9.0	EXP B-33	EXP B-38	EXP B-43	EXP B-48	EXP B-53	EXP B-58
13.5	EXP B-34	EXP B-39	EXP B-44	EXP B-49	EXP B-54	EXP B-59
18.0	EXP B-35	EXP B-40	EXP B-45	EXP B-50	EXP B-55	EXP B-60

Table 4-2b, One Buck Chopper Feeding Two Buck Choppers

	Light load on DC-DC1	Heavy load on DC-DC1
Line Inductance (μh)	DC-DC3 @ 50 Hz DC-DC4 @ 75 Hz	DC-DC3 @ 50 Hz DC-DC4 @ 75 Hz
0.0	EXP B-61	EXP B-66
4.5	EXP B-62	EXP B-67
9.0	EXP B-63	EXP B-68
13.5	EXP B-64	EXP B-69
18.0	EXP B-65	EXP B-70

Table 4-2c, One Buck Chopper Feeding Two Buck Choppers

3. Two Paralleled Buck Choppers Feeding One Buck Chopper

a. Topology

The basic testing topology used for this series of tests is shown in Figure (4-4). The resistance values used are as follows: $R_1 = 45\ \Omega$ (light loading), $R_1 = 7\ \Omega$ (heavy loading), $R_2 = 144\ \Omega$, $R_3 = 18\ \Omega$.

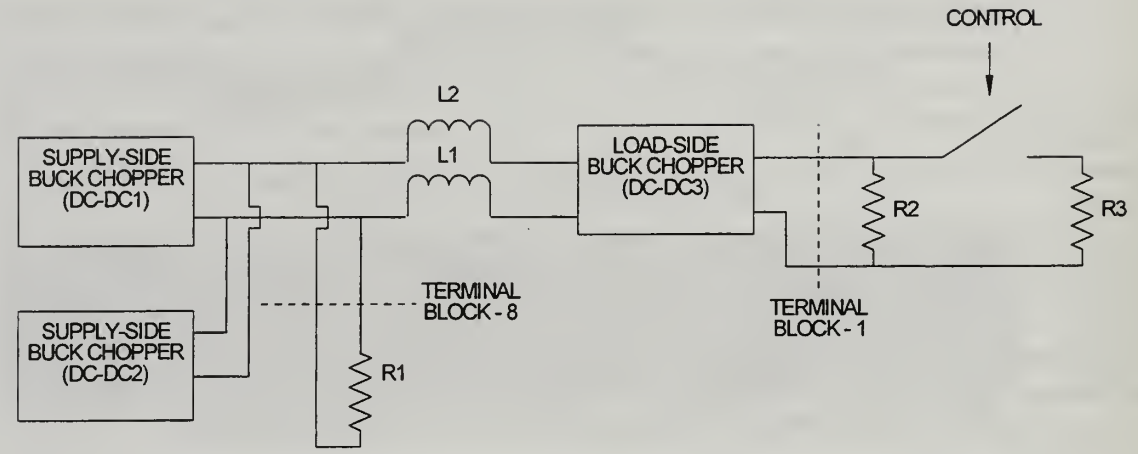

Figure 4-4, Topology Used For Two Buck Choppers Feeding One Buck Chopper

b. Line Inductance

The switching grid was manipulated to place line inductance between the two supply-side buck choppers (DC-DC1 & DC-DC2) and a load-side buck chopper (DC-DC3) in a manner similar to the simple series configuration: Starting with all contactors open, to place 0.0 μH of line inductance, contactors A-1, A-7, A-9 and A-11 were closed. To increase the line inductance to 4.5 μH, contactor A-7 A-9 and A-11 were opened and contactors A-8, A-10 and A-12 were closed. As before, a 9.0 μH line inductance was realized by placing RL-link 1 and RL-link 2 in series: A-8, A-10 and A-12 were opened and contactors B-8, B-10, B-12 and L-1 were closed. In a similar manner, B-8, B-10 and B-12 were opened and C-8, C-10, C-12 and L-2 were closed to provide 13.5 μH of line inductance. Finally, C-8, C-10 and C-12 were opened and D-8, D-10, D-12 and L-3 were closed to place all four RL links in series, providing 18.0μH of line inductance.

c. *Load-Side Buck Chopper Loading*

The procedure used in this phase was similar to the procedure used in the simple series test. The only variation was the presence of a second supply-side buck chopper. This had no effect on the test procedures used for the load-side buck chopper. Table (4-3) is a tabular representation of the testing performed in this phase. This phase of the research effort contains 30 separate experiments.

	Light load on DC-DC1 & DC-DC2			Heavy load on DC-DC1 & DC-DC2		
	DC-DC3			DC-DC3		
Line Inductance (μh)	10%→ 90%	90%→ 10%	Oscillation	10%→ 90%	90%→ 10%	Oscillation
0.0	EXP C-1	EXP C-6	EXP C-11	EXP C-16	EXP C-21	EXP C-26
4.5	EXP C-2	EXP C-7	EXP C-12	EXP C-17	EXP C-22	EXP C-27
9.0	EXP C-3	EXP C-8	EXP C-13	EXP C-18	EXP C-23	EXP C-28
13.5	EXP C-4	EXP C-9	EXP C-14	EXP C-19	EXP C-24	EXP C-29
18.0	EXP C-5	EXP C-10	EXP C-15	EXP C-20	EXP C-25	EXP C-30

Table 4-3, Two Paralleled Buck Choppers Feeding One Buck Chopper

4. Two Buck Choppers in Parallel Feeding Two Buck Choppers

a. *Topology*

The basic testing topology used for this series of tests is shown in Figure (4-5). The resistance values used are as follows: $R_1 = 45\ \Omega$ (light loading), $R_1 = 9\ \Omega$ (heavy loading), $R_2 = R_4 = 144\ \Omega$, $R_3 = R_5 = 18\ \Omega$.

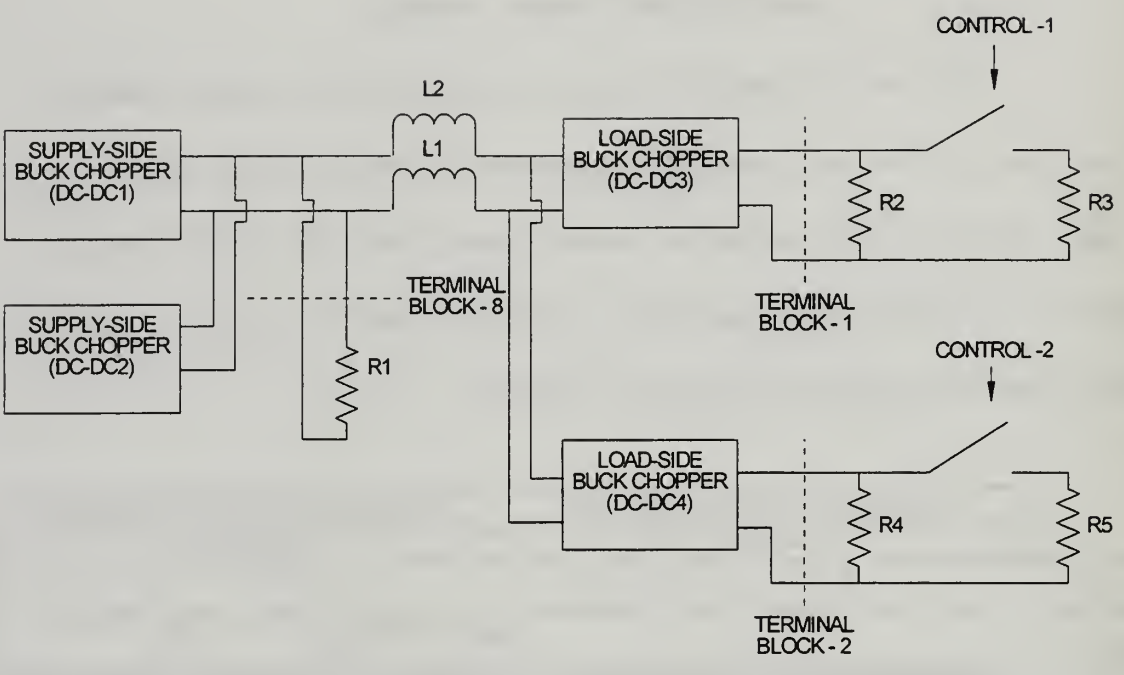

Figure 4-5, Topology Used For Two Buck Choppers Feeding Two Buck Choppers

b. Line Inductance

The switching grid was manipulated to place line inductance between the supply-side buck choppers (DC-DC1 & DC-DC2) and the two load-side buck choppers (DC-DC3 & DC-DC4). The procedure used in the series connection with two supply-side buck choppers described above was repeated with one variation, contactor A-2 was also closed in the initial setup and remained closed throughout this phase of the testing.

c. Load-Side Buck Chopper Loading

The procedure used in this phase was similar to the procedure used for the one supply-side buck chopper providing power to two load-side buck choppers. As before, DC-DC3 was again used to investigate system transients. The same three basic tests were performed as before, but with DC-DC4 operating at either a high or a low load

demand. Tables (4-4a) and (4-4b) are tabular representations of these tests. As described in a previous section, a non-synchronous variable load demand test was also performed. For this experiment, the load bank attached to DC-DC3 was fed the same control signal as before (50 Hz), but the load bank attached to DC-DC4 was fed a 75 Hz control signal. This was done at all five values of line inductance and for both supply-side buck chopper load demand conditions. Table (4-4c) encapsulates these procedures.

	DC-DC4 at 10% load					
	Light load on DC-DC1 & DC-DC2			Heavy load on DC-DC1 & DC-DC2		
	DC-DC3			DC-DC3		
Line Inductance (μh)	10%→ 90%	90%→ 10%	Oscillation	10%→ 90%	90%→ 10%	Oscillation
0.0	EXP D-1	EXP D-6	EXP D-11	EXP D-16	EXP D-21	EXP D-26
4.5	EXP D-2	EXP D-7	EXP D-12	EXP D-17	EXP D-22	EXP D-27
9.0	EXP D-3	EXP D-8	EXP D-13	EXP D-18	EXP D-23	EXP D-28
13.5	EXP D-4	EXP D-9	EXP D-14	EXP D-19	EXP D-24	EXP D-29
18.0	EXP D-5	EXP D-10	EXP D-15	EXP D-20	EXP D-25	EXP D-30

Table 4-4a, Two Buck Choppers Feeding Two Buck Choppers

	DC-DC4 at 90% load					
	Light load on DC-DC1 & DC-DC2			Heavy load on DC-DC1 & DC-DC2		
	DC-DC3			DC-DC3		
Line Inductance (μh)	10%→ 90%	90%→ 10%	Oscillation	10%→ 90%	90%→ 10%	Oscillation
0.0	EXP D-31	EXP D-36	EXP D-41	EXP D-46	EXP D-51	EXP D-56
4.5	EXP D-32	EXP D-37	EXP D-42	EXP D-47	EXP D-52	EXP D-57
9.0	EXP D-33	EXP D-38	EXP D-43	EXP D-48	EXP D-53	EXP D-58
13.5	EXP D-34	EXP D-39	EXP D-44	EXP D-49	EXP D-54	EXP D-59
18.0	EXP D-35	EXP D-40	EXP D-45	EXP D-50	EXP D-55	EXP D-60

Table 4-4b, Two Paralleled Buck Chopper Feeding Two Buck Choppers

	Light load on DC-DC1 & DC-DC2	Heavy load on DC-DC1 & DC-DC2
Line Inductance (μh)	DC-DC3 @ 50 Hz DC-DC4 @ 75 Hz	DC-DC3 @ 50 Hz DC-DC4 @ 75 Hz
0.0	EXP D-61	EXP D-66
4.5	EXP D-62	EXP D-67
9.0	EXP D-63	EXP D-68
13.5	EXP D-64	EXP D-69
18.0	EXP D-65	EXP D-70

Table 4-4c, Two Paralleled Buck Choppers Feeding Two Buck Choppers

This procedure contains 200 separate experiments designed to examine the interaction between devices. The ability of the testbed to be quickly reconfigured will also be verified in these experiments, as will be the general validity of the DC ZEDS concept. Chapter V, Experimental Results, contains the analysis of the information obtained in these experiments. Additionally, a discussion of the standards and criteria used in the acquisition of data is contained in Chapter V.

V. EXPERIMENTAL RESULTS

A. INTRODUCTION

This chapter summarizes the results of the 200 experiments conducted to support this research endeavor. A brief description of the test equipment used and a discussion of the harmonics and noise levels associated with the source-side and load-side buck choppers are followed by a breakdown of the experiments by testing topology. The results for each topology examined are broken down into five subsections: a discussion of the noise levels observed on the network, the results of the three basic experiments on the load-side buck chopper(s) and a brief analysis of the trends found in the data.

As discussed in the previous chapter, the three basic experiments consist of step changes from light to heavy load, step changes from heavy to light load, and periodic step changes in load. The light to heavy load transition is defined as a step increase from 10% to 90% of the rated capacity in the load demand on the load-side buck chopper. The heavy to light load transition is defined as a step decrease from 90% to 10% of the rated capacity in the load demand on the load-side buck chopper. The oscillating load condition is a periodic cycling, normally at 50 Hz, between 10% to 90% of the rated capacity of the load-side buck chopper.

B. TEST EQUIPMENT, TERMINOLOGY AND DEVICE NOISE LEVELS

1. Test Equipment

Multiple test devices were used to assist in gathering data in these experiments. Table (5-1) lists the manufacturer and model number information for the test equipment utilized.

DEVICE (QUANTITY)	MANUFACTURER	MODEL NUMBER
OSCILLISCOPE (2)	TEKTRONIX	(1) TDS540 (1) TDS420
VOLTAGE ISOLATOR (4)	TEKTRONIX	P5200
CURRENT PROBE (4)	TEKTRONIX	A6303
CURRENT PROBE AMP (4)	TEKTRONIX	AM503A
DIGITAL MULTIMETER (2)	TEKTRONIX	DM2510
DIGITAL MULTIMETER (2)	FLUKE	8060A

Table 5-1, Test Equipment

2. Terminology

The transient response characteristics observed and reported on in this research are graphically displayed in Figure (5-1a) and Figure (5-1b). The terms are defined as follows:

- Steady-State - Condition where the measured level remains within the noise band.
- Noise Level (band) - The peak-to-peak noise ripple on a measured signal.
- Spike - In AC coupled signals, the initial response to a transient on a measured signal.
- Overshoot - Condition where the response to a transient initially exceeds the final steady-state value before settling at that value.

- Settling Time - Time between the introduction of a transient and the measured value assuming a steady-state condition.

In most circumstances, current measurements were taken with DC coupling, and voltage measurements were taken using AC coupling. This was done for clarity and scale purposes. The transient is more readily observed in a DC coupled current display and the relative scale of the steady-state values to the disturbance values is approximately one order of magnitude. The voltage data is collected using AC coupling primarily due to the fact that the disturbance values are commonly two orders of magnitude lower than the steady-state value; if DC coupling was used for these measurements, there would be no observable variation in voltage levels

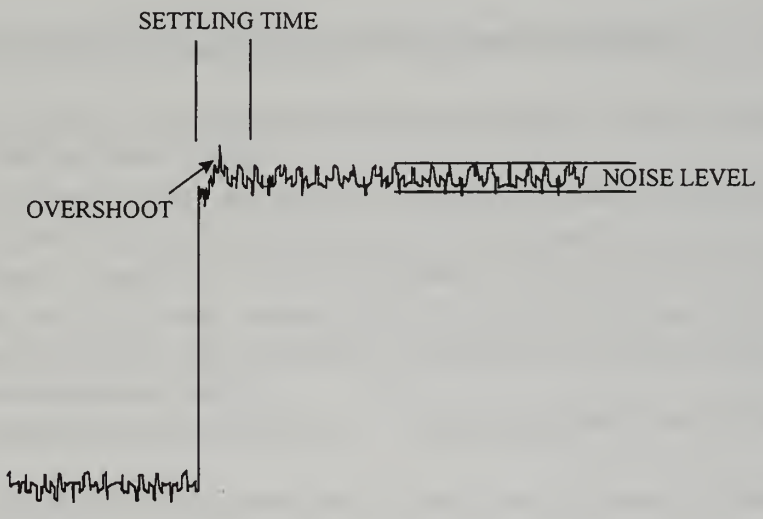

Figure 5-1a, Terminology Example , DC Coupling

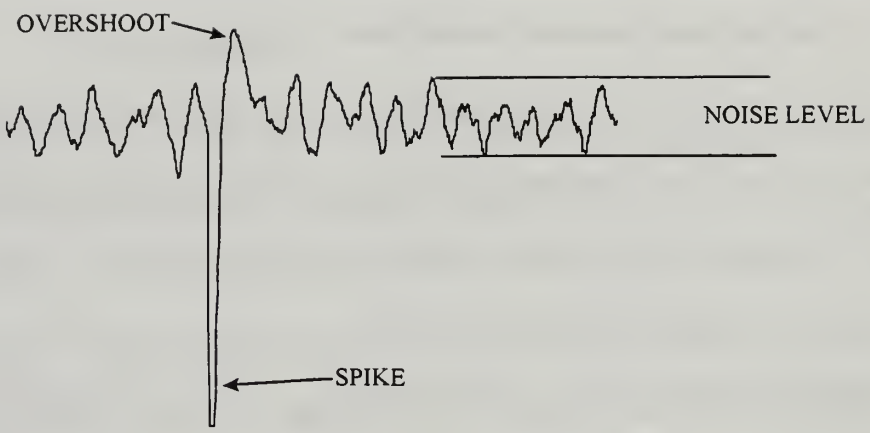

Figure 5-1b, Terminology Example , AC Coupling

3. Device Noise Levels

Badorf [5] states that the output peak-to-peak voltage ripple for both the source-side and the load-side buck choppers operating individually with a fixed load is not greater than one percent. This corresponds to a three volt ripple on the source-side buck choppers and a two volt ripple on the load side devices. The output voltage ripple of all four test devices was verified by stand-alone testing over the complete power range of the devices and found to be within this tolerance. A similar test was performed on each topology examined to determine the noise levels on the network. A discussion of the noise levels for each network configuration is included with the results for that configuration.

Noise and harmonics are introduced into the network from a myriad of sources. Stray inductance, stray capacitance, switching effects and organic noise in the measuring devices all contribute to the noise levels observed. These noise levels may be

significantly attenuated by the introduction of additional capacitance at the various load busses. The rationale for not placing additional capacitance on the network was multi-faceted. First, the purpose of this research is to examine the effects of the interconnection of buck converters; noise and harmonics introduced by this interconnection are key parameters of interest. Second, the presence of additional capacitance would slow, or even completely mask, the response of the system to a transient; the system response to a transient is another central feature of this research. Lastly, we are attempting to model a ship-board scale DC ZEDS architecture; placing significant amounts of additional capacitance on an actual ship-board network would require a prohibitive amount of weight and volume using current technology capacitors.

C. ONE BUCK CHOPPER FEEDING ONE BUCK CHOPPER

1. Device Noise Levels

When the source-side and load-side devices were connected in series, with the load-side converter supplying static resistive loads, the output noise levels were unchanged from the stand-alone testing.

2. Light Load to Heavy Load

In this simple series topology changing the line inductance appeared to influence only one of the step response characteristics: the bus voltage settling time slightly decreased as line inductance between the source-side and load-side buck choppers was increased for the lightly loaded source-side buck chopper condition. Some effects were also seen when the source-side buck chopper load level was changed. The bus current

overshoot was higher and the load voltage settling time was slightly longer with a light load on the source-side converter. Figures (5-2a) through (5-2d) are typical output oscillograms for this series of experiments. These plots were taken with a light source-side buck chopper load demand and 0.0 μH of line inductance inserted between the source-side and load-side buck choppers. The oscillogram was obtained using the data capture mode of the oscilloscope. This mode allows data in ASCII format to be transferred from the oscilloscope to a personal computer via an IEEE 488 interface. Table (5-2) summarizes the data collected in this set of experiments. The difference in the bus voltage steady-state value at the different source-side buck chopper load levels is caused by the house curve inserted into the analog control system on the source-side buck choppers (see Badorf [5]).

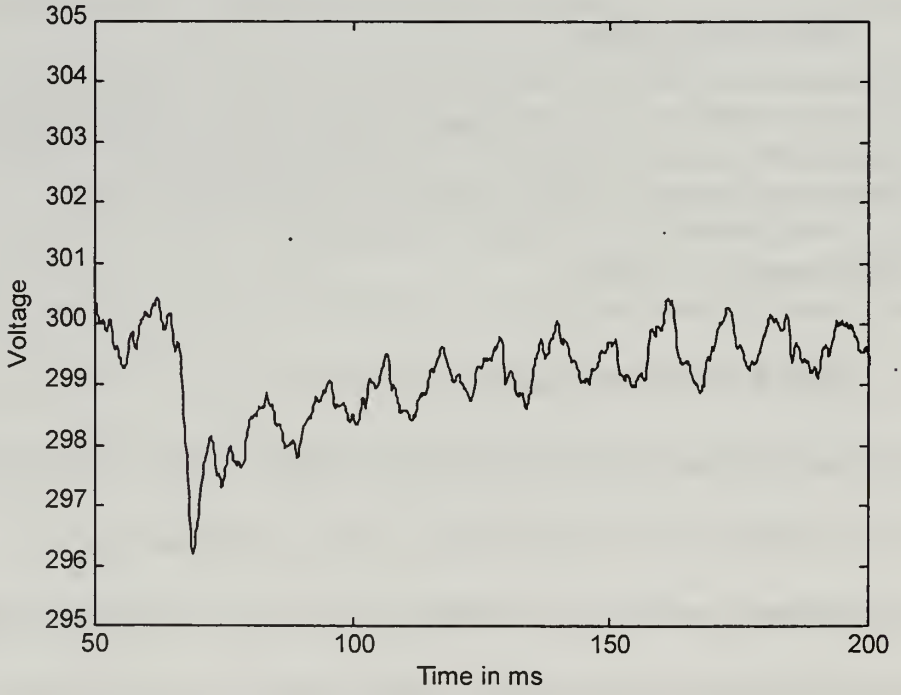

Figure 5-2a, Output Voltage Oscillogram, DC-DC1

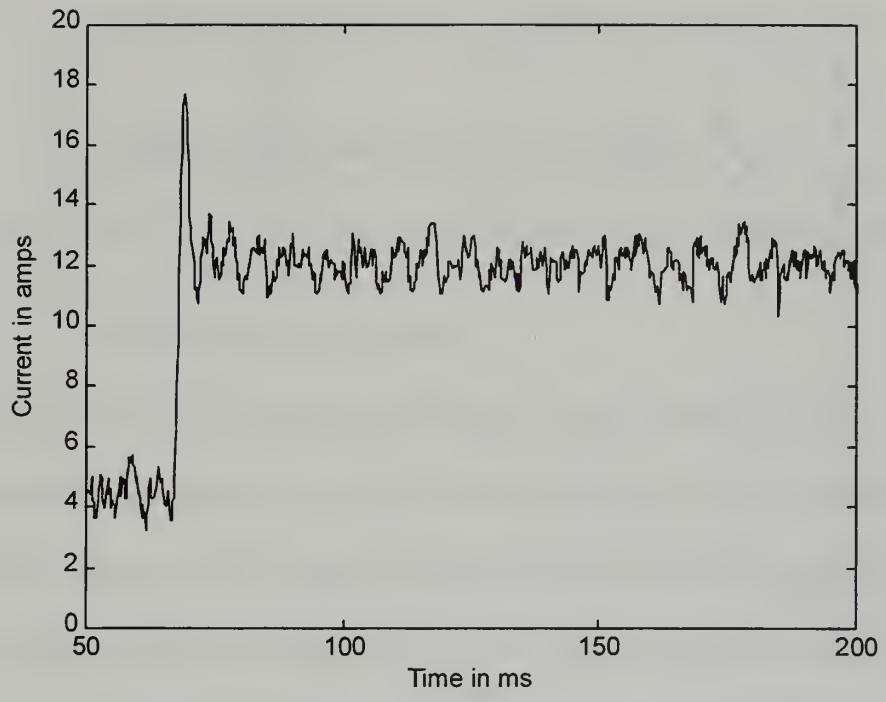

Figure 5-2b, Output Current Oscillogram, DC-DC1

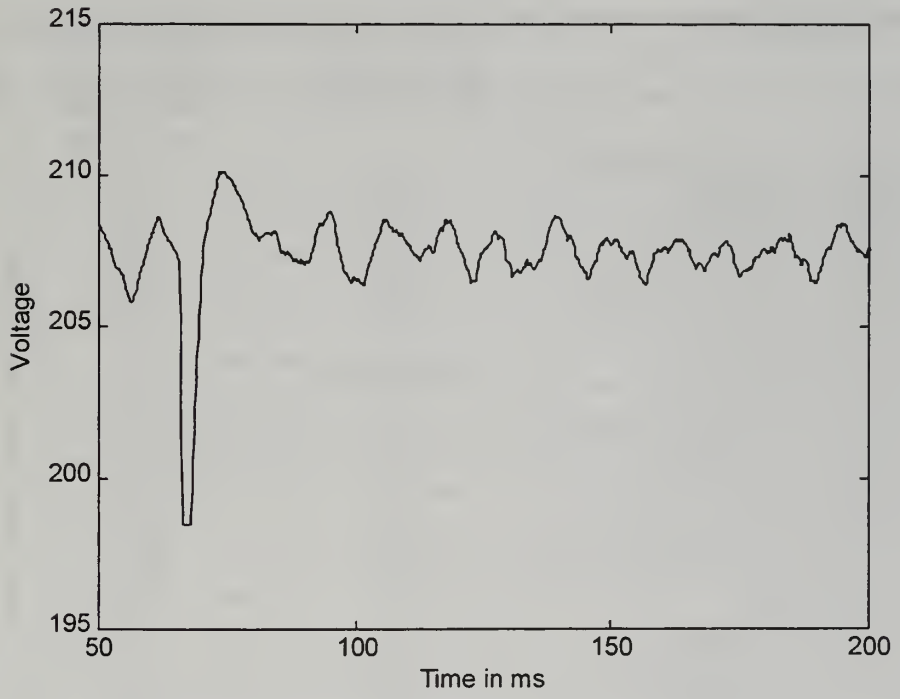

Figure 5-2c, Output Voltage Oscillogram, DC-DC3

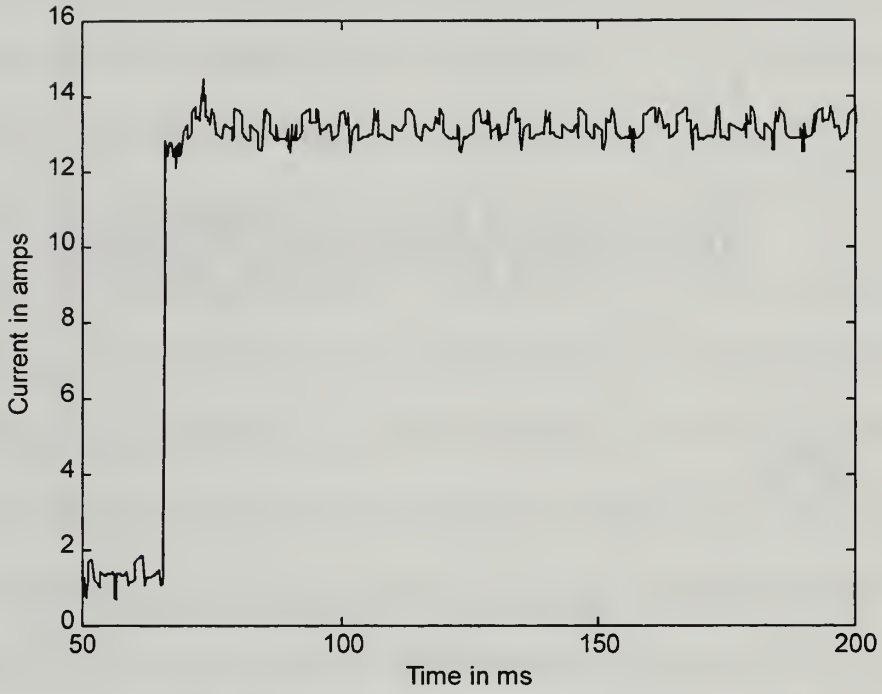

Figure 5-2d, Output Current Oscillogram, DC-DC3

PARAMETER	LIGHT LOAD ON SOURCE-SIDE DEVICE (A1-A5)	HEAVY LOAD ON SOURCE-SIDE DEVICE (A16-A20)
BUS CURRENT AT STEADY STATE	12.0 A	26.3 A
BUS CURRENT OVERSHOOT	6.6 A	4.0 A
BUS CURRENT SETTLING TIME	3 ms	5 ms
BUS CURRENT NOISE LEVEL	0.2 A	1.0 A
BUS VOLTAGE AT STEADY STATE	299 V	298 V
BUS VOLTAGE OVERSHOOT	5 V	5 V
BUS VOLTAGE SETTLING TIME	See Table 5-2a	25 ms
BUS VOLTAGE NOISE LEVEL	2 V	2 V
LOAD CURRENT AT STEADY STATE	13.3 A	13.3 A
LOAD CURRENT OVERSHOOT	0.2 A	0.2 A
LOAD CURRENT SETTLING TIME	10 ms	10 ms
LOAD CURRENT NOISE LEVEL	0.1 A	0.1 A
LOAD VOLTAGE AT STEADY STATE	208 V	208 V
LOAD VOLTAGE SPIKE	9 V	9 V
LOAD VOLTAGE OVERSHOOT	7 V	5 V
LOAD VOLTAGE SETTLING TIME	15 ms	10 ms
LOAD VOLTAGE NOISE LEVEL	2 V	2 V

Table 5-2, Series A, Light to Heavy Load on Load-Side Buck Chopper

LINE INDUCTANCE - μH	SETTLING TIME - ms
0.0	30
4.5	30
9.0	30
13.5	20
18.0	20

Table 5-2a, Line Inductance - Bus Voltage Settling Time Relationship

3. Heavy Load to Light Load

In this set of tests, the transient performance figures of merit observed were almost constant under changes to source-side converter loading and line inductance with one exception; again, the bus voltage settling time under a light source-side buck chopper load decreased from 50ms to 20ms as line inductance was increased (see Table (5-3a)). Figures (5-3a) through (5-3d) are typical output oscillograms for this series of experiments. As before, these plots were taken with a light source-side buck chopper load demand and 0.0 μH of line inductance inserted between the source-side and load-side buck choppers. Table (5-3) summarizes the data obtained in this portion of the procedure.

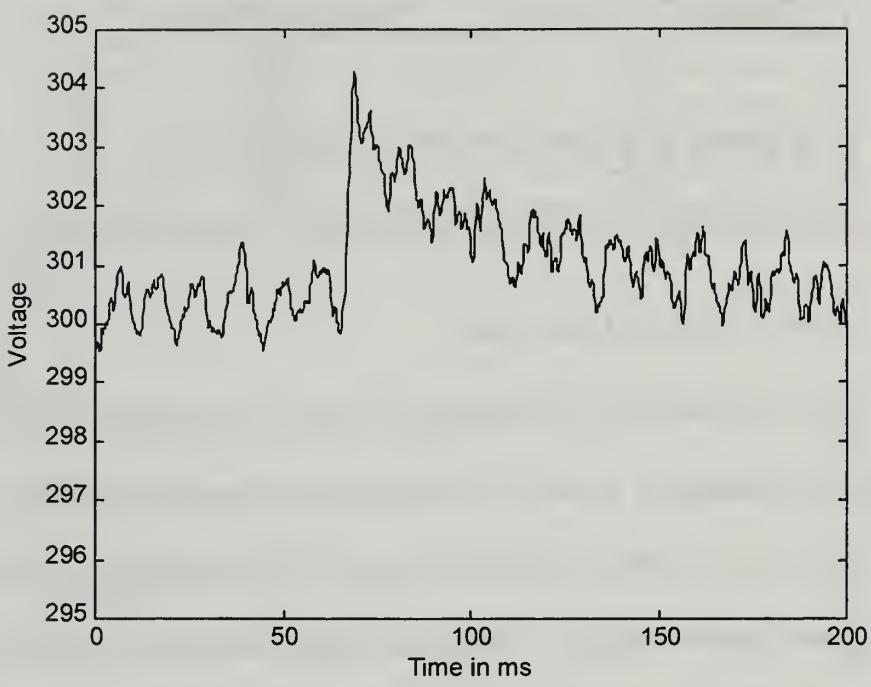

Figure 5-3a, Output Voltage Oscillogram, DC-DC1

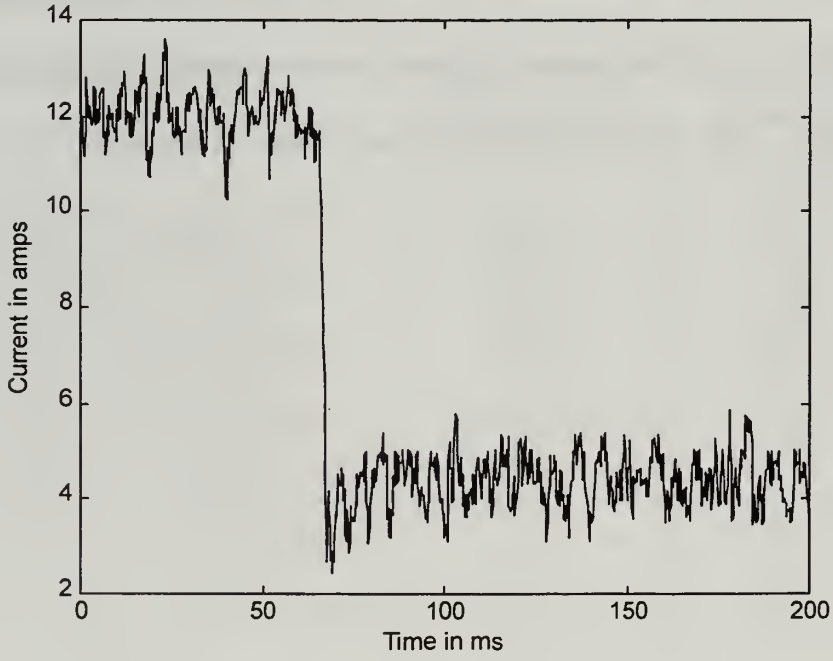

Figure 5-3b, Output Current Oscillogram, DC-DC1

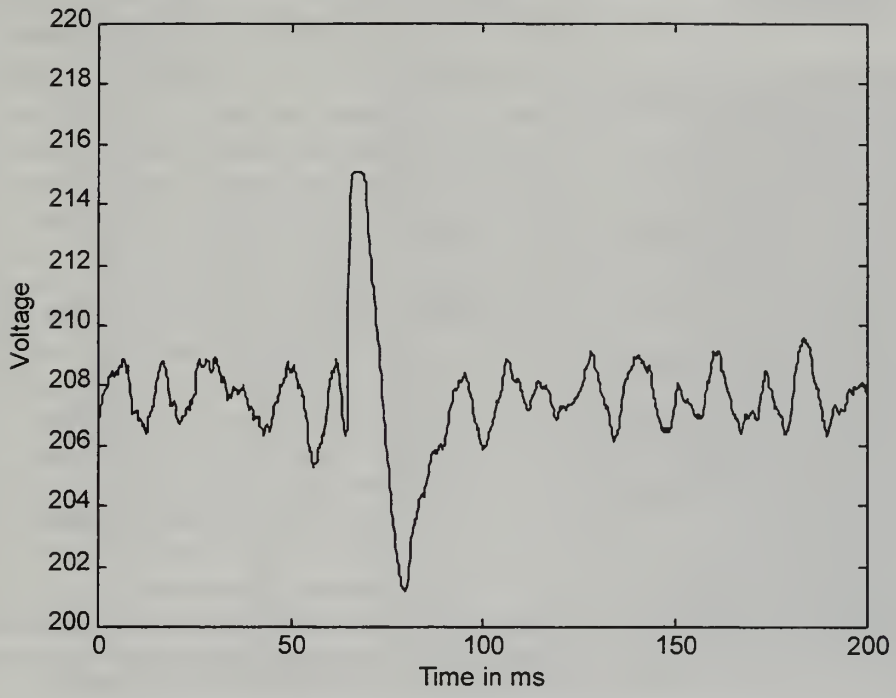

Figure 5-3c, Output Voltage Oscillogram, DC-DC3

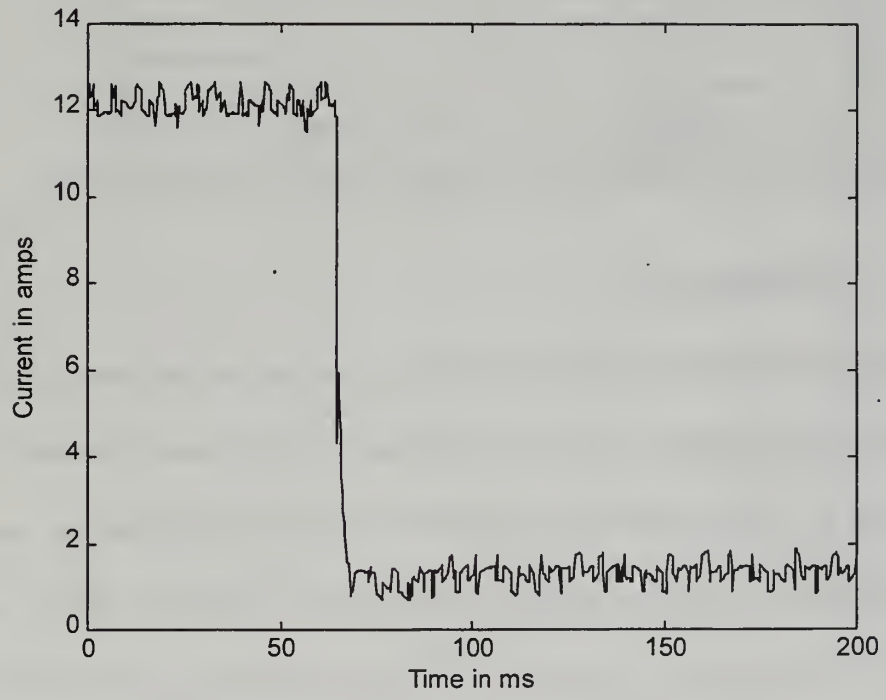

Figure 5-3d, Output Current Oscillogram, DC-DC3

PARAMETER	LIGHT LOAD ON SOURCE-SIDE DEVICE (A6-A10)	HEAVY LOAD ON SOURCE-SIDE DEVICE (A21-A25)
BUS CURRENT AT STEADY STATE	4.3 A	18.6 A
BUS CURRENT OVERSHOOT	3.4	4.0 A
BUS CURRENT SETTLING TIME	10 ms	10 ms
BUS CURRENT NOISE LEVEL	0.2 A	1.0 A
BUS VOLTAGE AT STEADY STATE	301 V	300 V
BUS VOLTAGE OVERSHOOT	5 V	5 V
BUS VOLTAGE SETTLING TIME	See Figure (5-3a)	20 ms
BUS VOLTAGE NOISE LEVEL	2 V	2 V
LOAD CURRENT AT STEADY STATE	1.4 A	1.4 A
LOAD CURRENT OVERSHOOT	0.2 A	0.2 A
LOAD CURRENT SETTLING TIME	15 ms	15 ms
LOAD CURRENT NOISE LEVEL	0.1 A	0.1 A
LOAD VOLTAGE AT STEADY STATE	208 V	208 V
LOAD VOLTAGE SPIKE	9 V	9 V
LOAD VOLTAGE OVERSHOOT	7 V	5 V
LOAD VOLTAGE SETTLING TIME	15 ms	15 ms
LOAD VOLTAGE NOISE LEVEL	2 V	2 V

Table 5-3, Series A, Heavy to Light Load on Load-Side Buck Chopper

LINE INDUCTANCE - μH	SETTLING TIME - ms
0.0	50
4.5	45
9.0	30
13.5	25
18.0	20

Table 5-3a, Line Inductance - Bus Voltage Settling Time Relationship

4. Oscillating Load

When the network was operated with cycled step changes in load power at a 50 Hz rate, the load voltage displayed a significant increase in peak-to-peak noise level. In these experiments, the peak-to-peak combination of voltage noise and harmonics were 15 volts under a light source-side converter load condition and 25 volts under a heavy load condition. All other values were consistent with the earlier experiments. Figure (5-4a) and Figure (5-4b) are the voltage and current oscillograms for the heavy (5 kW static load) source-side buck chopper loading level.

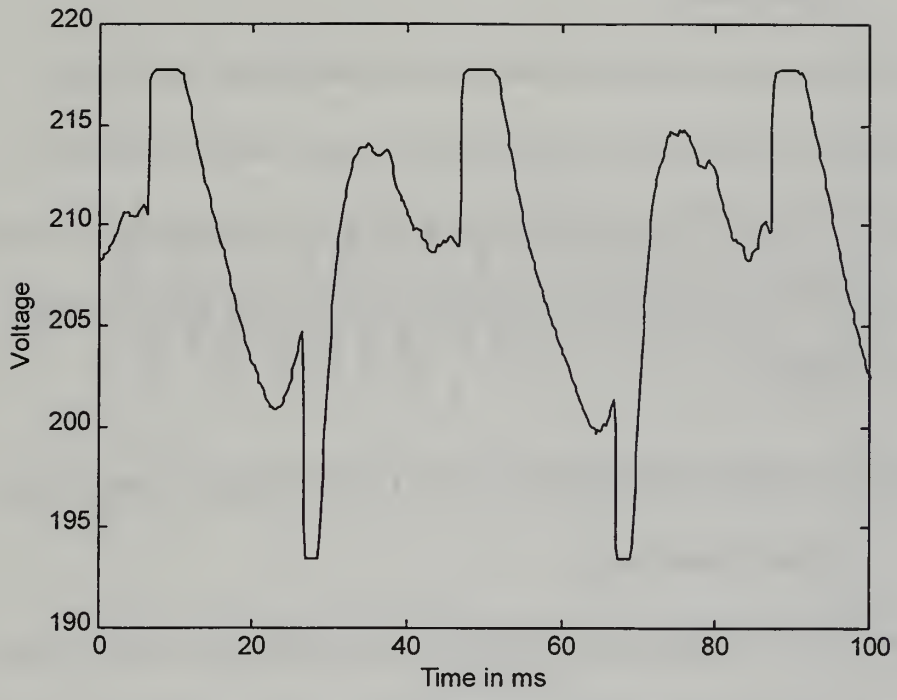

Figure 5-4a, Output Voltage Oscillogram, DC-DC3

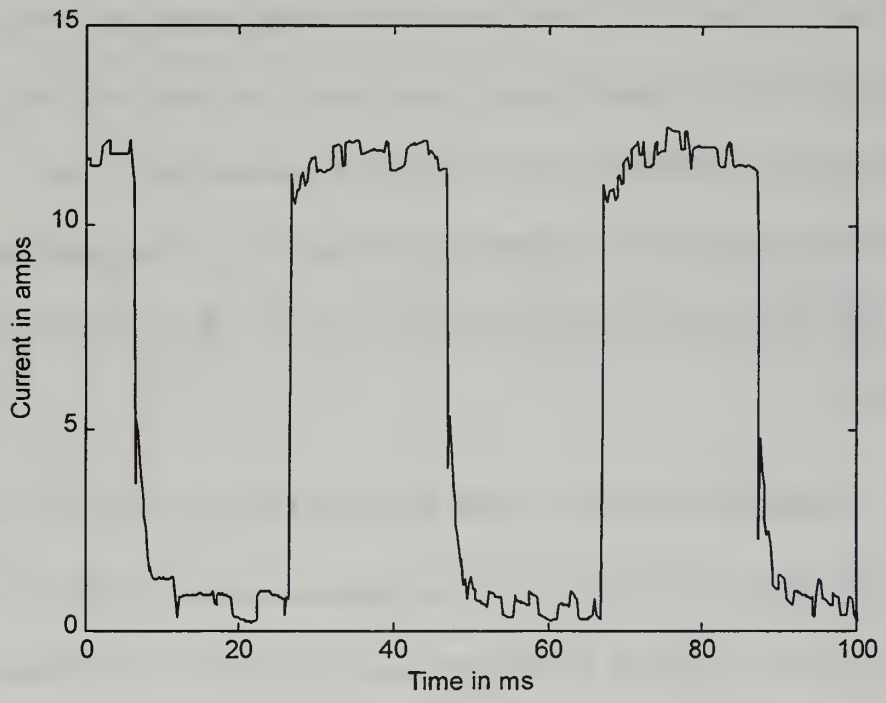

Figure 5-4b, Output Current Oscillogram, DC-DC3

5. Observations

In this series of experiments we observed three phenomena: bus current overshoot decreased with increased source-side buck chopper loading in the light to heavy load transition, bus voltage settling time decreased with increased line inductance under a light source-side buck chopper load, and the noise band increased during the oscillating load condition.

D. ONE BUCK CHOPPER FEEDING TWO CHOPPERS IN PARALLEL

1. Device Noise Levels

As stated earlier in this section, the output noise level of each test device were confirmed to be approximately one percent in stand-alone testing. When the two load-side buck choppers were tied to a common input bus, the resulting output had a two percent (4 volts) peak-to-peak ripple. The output noise level of the source-side buck chopper was unchanged and remained at approximately one percent peak-to-peak. These noise levels are documented in Figures (5-5a) through (5-5c). These oscillograms were taken at a light source-side buck chopper load with a 10% load on each of the load-side buck choppers.

2. Effect of Transients on Load-Side Buck Chopper with Static Load

In 60 of the experiments in this series, a load-side buck chopper, DC-DC4, was used to supply a static resistive load. In these experiments, there were no observable effects on the performance characteristics of this device.

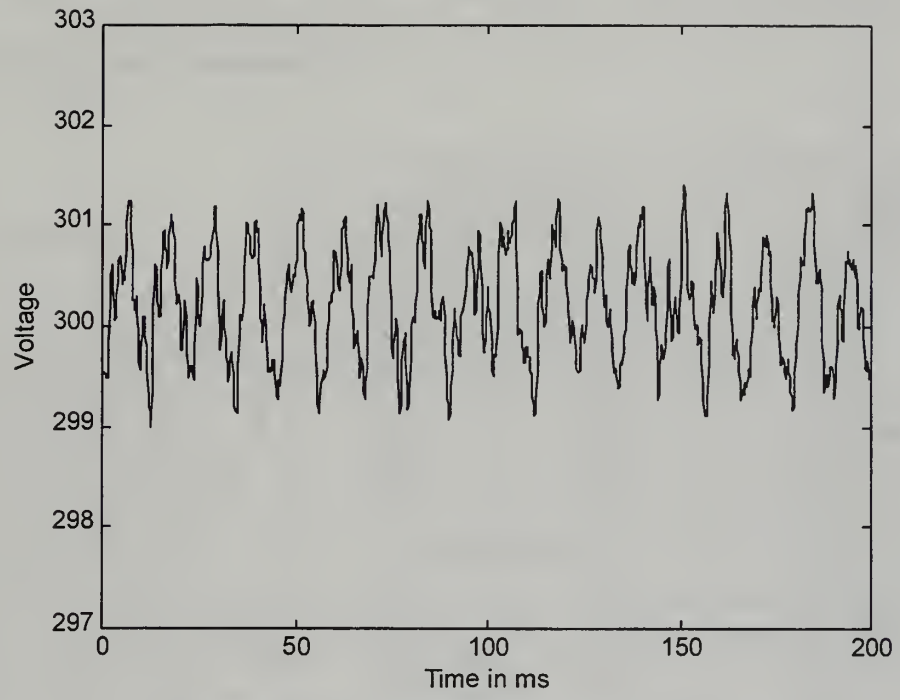

Figure 5-5a, Output Voltage Ripple, DC-DC1

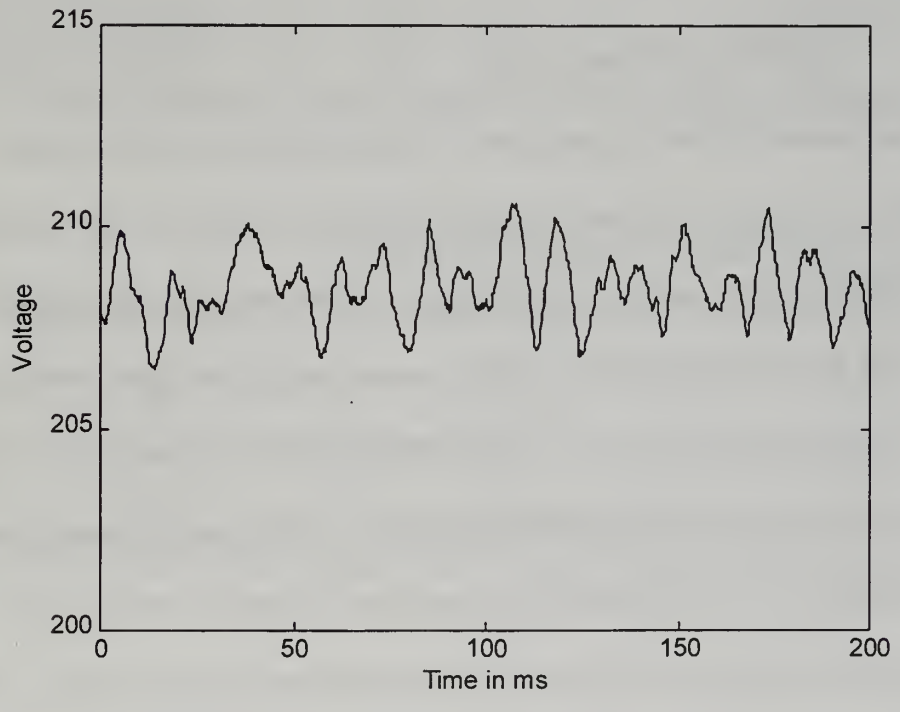

Figure 5-5b, Output Voltage Ripple, DC-DC3

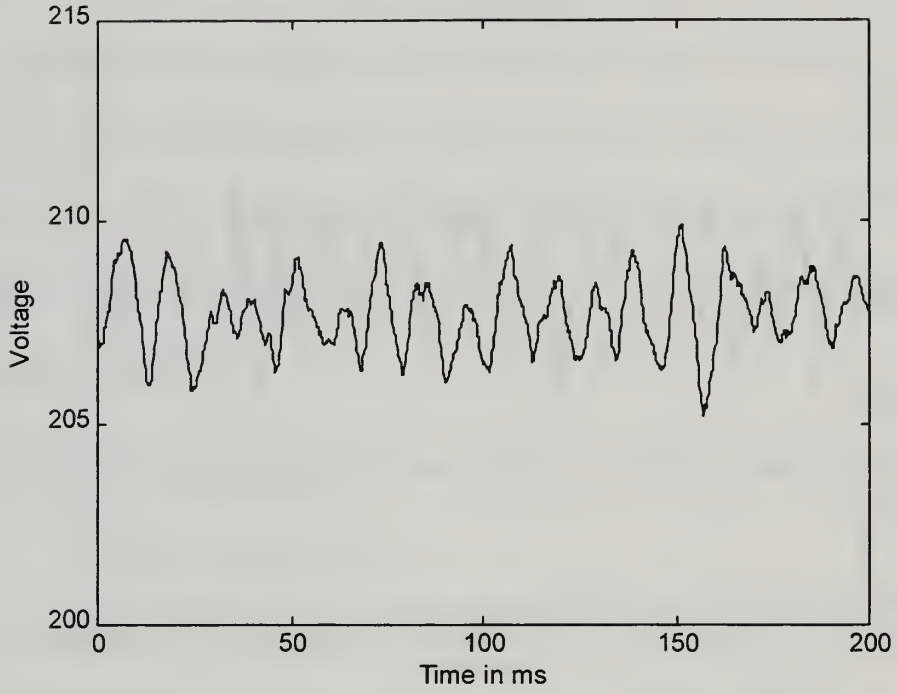

Figure 5-5c, Output Voltage Ripple, DC-DC4

3. Light Load to Heavy Load

The data acquired in these experiments virtually mirrored the results from the previous section. Again the bus voltage settling time slightly decreased as line inductance was increased for the lightly loaded source-side buck chopper condition. This effect was consistent at both levels of load-side buck chopper static loading. The slight changes in bus current overshoot and settling time were not observed; the bus current overshoot and settling times were uniform throughout these experiments. The most significant finding in this set of experiments involved identifying the absence of voltage overshoot and settling time on output of the load-side buck chopper supplying the transient load. At the heavy load demand level of the source-side buck chopper, as well as on the heavy static load-side buck chopper load with a light source-side buck chopper load, there was no

overshoot observed at increased line inductance levels. Table (5-4) summarizes the data collected in this set of experiments.

PARAMETER	LIGHT LOAD ON SOURCE-SIDE DEVICE		HEAVY LOAD ON SOURCE-SIDE DEVICE	
	10% LOAD ON DC-DC4 (B1-B5)	90% LOAD ON DC-DC4 (B31-B35)	10% LOAD ON DC-DC4 (B16-B20)	90% LOAD ON DC-DC4 (B46-B50)
BUS CURRENT AT STEADY STATE	13.0 A	20.7 A	20.4 A	28.1 A
BUS CURRENT OVERSHOOT	2.0 A	2.0 A	2.0 A	2.0 A
BUS CURRENT SETTLING TIME	10 ms	10 ms	10 ms	10 ms
BUS CURRENT NOISE LEVEL	0.5 A	0.5 A	0.5 A	0.5 A
BUS VOLTAGE AT STEADY STATE	299 V	299 V	298 V	298 V
BUS VOLTAGE OVERSHOOT	4 V	4 V	4 V	4 V
BUS VOLTAGE SETTLING TIME	See Table 5-4a		25 ms	20 ms
BUS VOLTAGE NOISE LEVEL	2 V	2 V	2 V	2 V
LOAD CURRENT AT STEADY STATE	13.3 A	13.3 A	13.3 A	13.3 A
LOAD CURRENT OVERSHOOT	0.1 A	0.1 A	0.1 A	0.1 A
LOAD CURRENT SETTLING TIME	10 ms	10 ms	10 ms	10 ms
LOAD CURRENT NOISE LEVEL	0.1 A	0.1 A	0.1 A	0.1 A
LOAD VOLTAGE AT STEADY STATE	208 V	208 V	208 V	208 V
LOAD VOLTAGE SPIKE	10 V	10 V	10 V	10 V
LOAD VOLTAGE OVERSHOOT	3 V	See Table 5-4b		
LOAD VOLTAGE SETTLING TIME	5 ms	See Table 5-4b		
LOAD VOLTAGE NOISE LEVEL	4 V	4 V	4 V	4 V

Table 5-4, Series B, Light to Heavy Load on Load-Side Buck Chopper

LINE INDUCTANCE - μH	10% LOAD ON DC-DC4 (B1-B5) SETTLING TIME - ms	90% LOAD ON DC-DC4 (B31-B35) SETTLING TIME - ms
0.0	25	20
4.5	20	15
9.0	20	10
13.5	15	10
18.0	15	10

Table 5-4a, Line Inductance - Bus Voltage Settling Time Relationship

	LIGHT LOAD ON DC-DC1		HEAVY LOAD ON DC-DC1			
	HEAVY LOAD ON DC-DC4 (B16-B20)		LIGHT LOAD ON DC-DC4 (B31-B35)		HEAVY LOAD ON DC-DC4 (B46-B50)	
LINE INDUCTANCE - μH	OVERSHOOT - V	SETTLING TIME - ms	OVERSHOOT - V	SETTLING TIME - ms	OVERSHOOT - V	SETTLING TIME - ms
0.0	5	15	5	15	5	15
4.5	0	5	5	10	0	5
9.0	0	5	0	5	0	5
13.5	0	5	0	5	0	5
18.0	0	5	0	5	0	5

Table 5-4b, Line Inductance - Load Voltage Overshoot/Settling Time Relationship

4. Heavy Load to Light Load

As in the light load to heavy load experiments reported on above, the data acquired in this set of tests was almost identical to the results of the Series "A" experiments. As observed before, the bus voltage settling time under a light source-side buck chopper load decreased slightly as line inductance was increased. Table (5-5) summarizes the data obtained in these tests.

5. Oscillating Load

With the single oscillating load on one of the load-side converters, the performance characteristics were consistent with the Series "A" experiments. The peak-to-peak voltage noise was 20 volts under light source-side converter load conditions and 25 volts under voltage heavy load conditions. When the double oscillating load was introduced, DC-DC3 at 50 Hz and DC-DC4 at 75 Hz, large ripples appeared on the bus current and voltage as well as both load-side buck chopper outputs. The bus voltage assumed a triangle waveform-like shape with a 10 volt peak-to-peak range. The bus current also began to oscillate in a jagged waveform with a 15 amp peak-to-peak ripple. The 75 Hz load assumed a 50 volt peak-to-peak ripple and the 50 Hz load maintained a

20 volt ripple as in the single oscillation experiments. Oscillograms for these experiments can be found in Figures (5-6a) through (5-6f).

PARAMETER	LIGHT LOAD ON SOURCE-SIDE DEVICE		HEAVY LOAD ON SOURCE-SIDE DEVICE	
	10% LOAD ON DC-DC4 (B6-B10)	90% LOAD ON DC-DC4 (B36-B40)	10% LOAD ON DC-DC4 (B21-B26)	90% LOAD ON DC-DC4 (B51-B55)
BUS CURRENT AT STEADY STATE	5.3 A	13.0 A	12.7 A	20.4 A
BUS CURRENT OVERSHOOT	1.0 A	1.0 A	1.0 A	1.0 A
BUS CURRENT SETTLING TIME	10 ms	10 ms	10 ms	10 ms
BUS CURRENT NOISE LEVEL	0.5 A	0.5 A	0.5 A	0.5 A
BUS VOLTAGE AT STEADY STATE	301 V	301 V	301 V	301 V
BUS VOLTAGE OVERSHOOT	4 V	4 V	4 V	4 V
BUS VOLTAGE SETTLING TIME	See Table 5-5a		20 ms	20 ms
BUS VOLTAGE NOISE LEVEL	2 V	2 V	2 V	2 V
LOAD CURRENT AT STEADY STATE	1.5 A	1.5 A	1.5 A	1.5 A
LOAD CURRENT OVERSHOOT	0.1 A	0.1 A	0.1 A	0.1 A
LOAD CURRENT SETTLING TIME	15 ms	15 ms	15 ms	15 ms
LOAD CURRENT NOISE LEVEL	0.1 A	0.1 A	0.1 A	0.1 A
LOAD VOLTAGE AT STEADY STATE	208 V	208 V	208 V	208 V
LOAD VOLTAGE SPIKE	10 V	10 V	10 V	10 V
LOAD VOLTAGE OVERSHOOT	5 V	5 V	5 V	5 V
LOAD VOLTAGE SETTLING TIME	15 ms	15 ms	15 ms	15 ms
LOAD VOLTAGE NOISE LEVEL	4 V	4 V	4 V	4 V

Table 5-5, Series B, Heavy to Light Load on Load-Side Buck Chopper

	10% LOAD ON DC-DC4 (B6-B10)	90% LOAD ON DC-DC4 (B31-B35)
LINE INDUCTANCE - μH	SETTLING TIME - ms	SETTLING TIME - ms
0.0	40	30
4.5	30	20
9.0	25	15
13.5	20	10
18.0	10	10

Table 5-5a, Line Inductance - Bus Voltage Settling Time Relationship

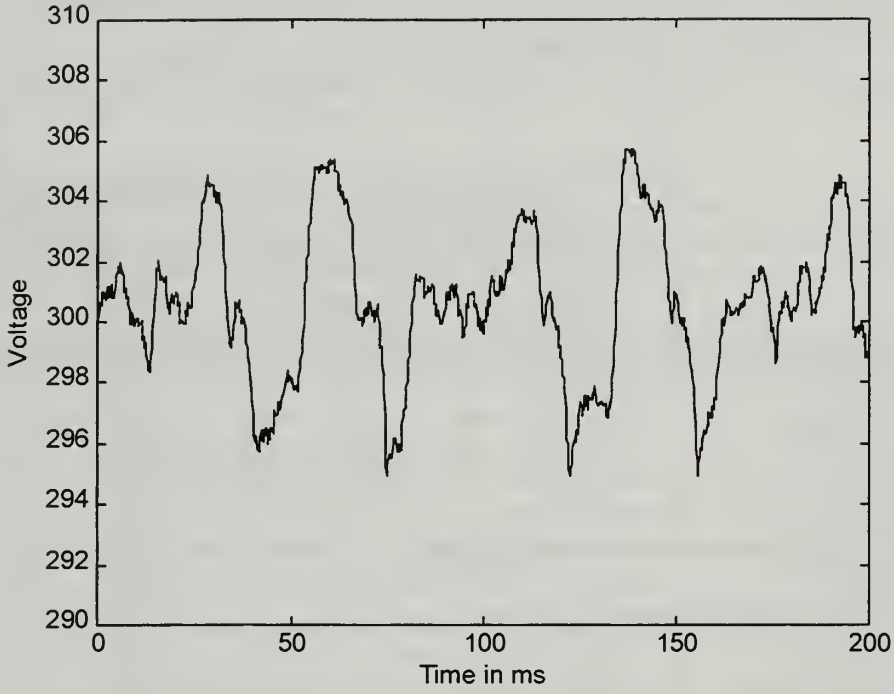

Figure 5-6a, Output Voltage Oscillogram, DC-DC1

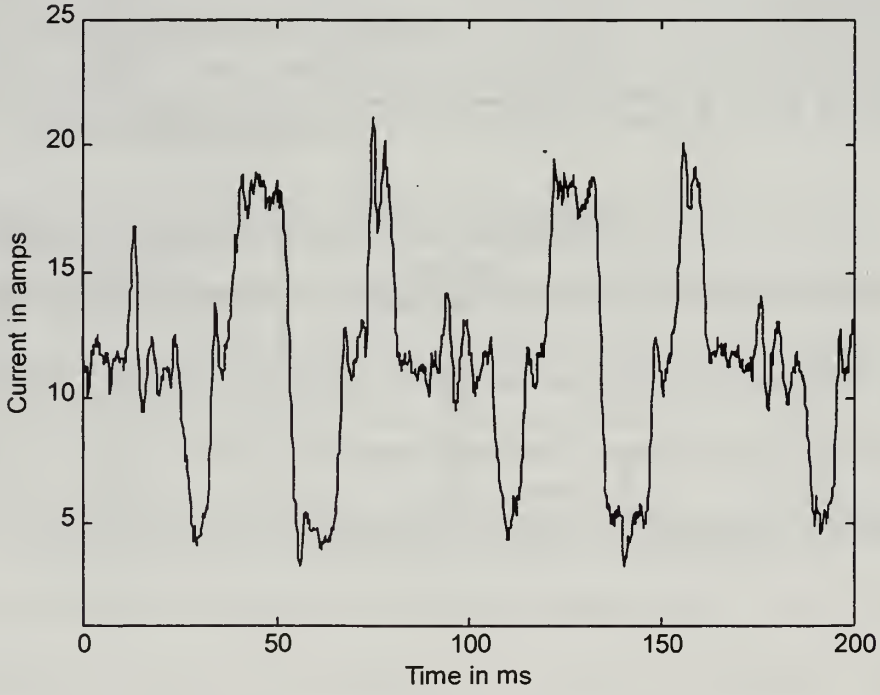

Figure 5-6b, Output Current Oscillogram, DC-DC1

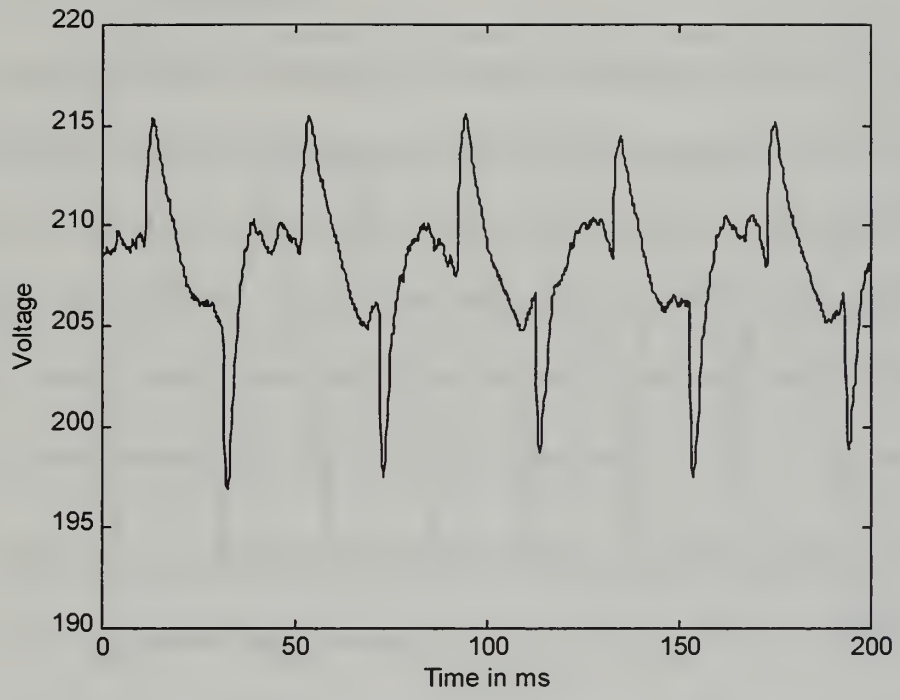

Figure 5-6c, Output Voltage Oscillogram, DC-DC3

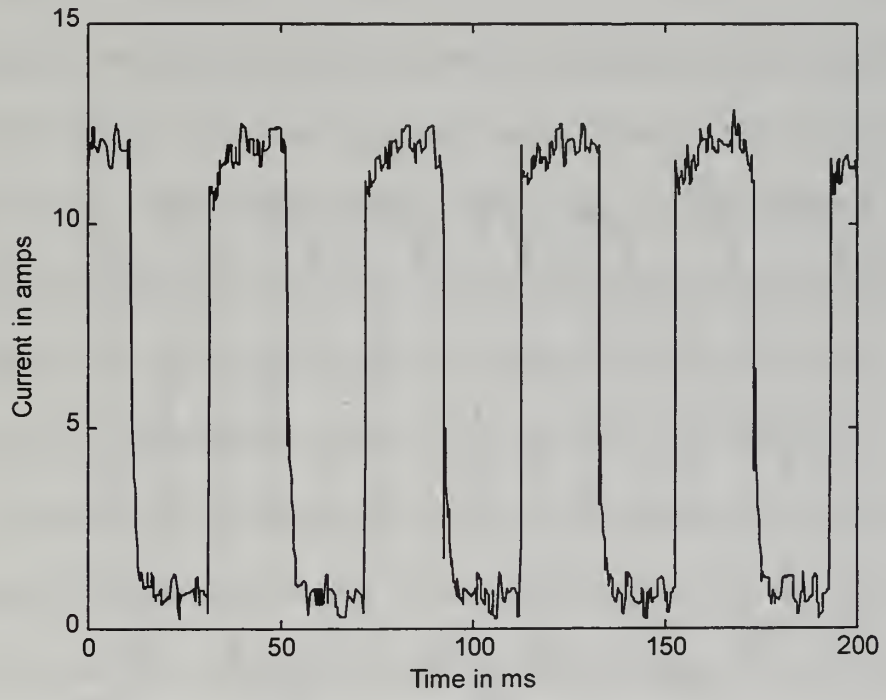

Figure 5-6d, Output Current Oscillogram, DC-DC3

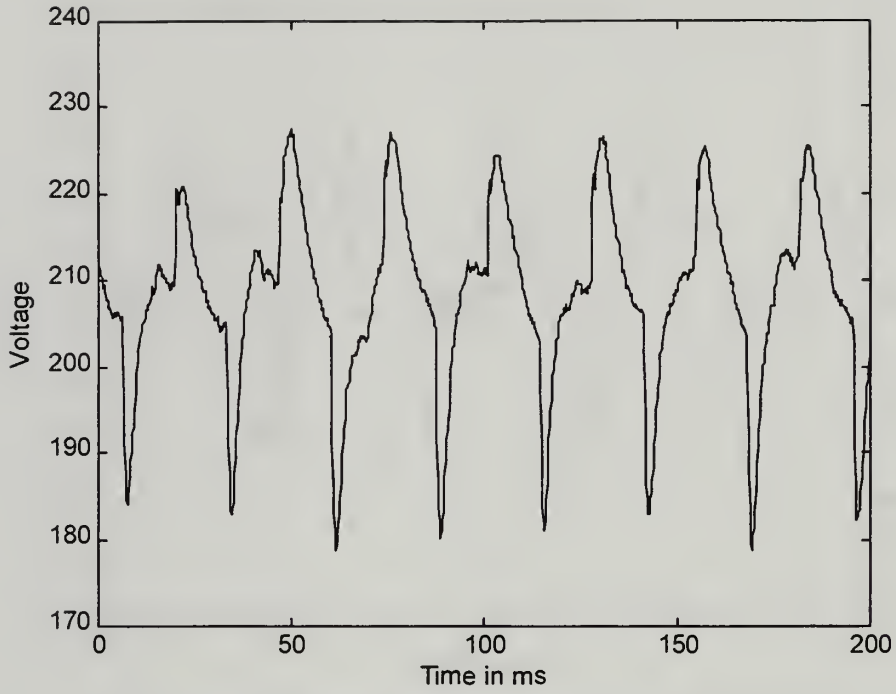

Figure 5-6e, Output Voltage Oscillogram, DC-DC4

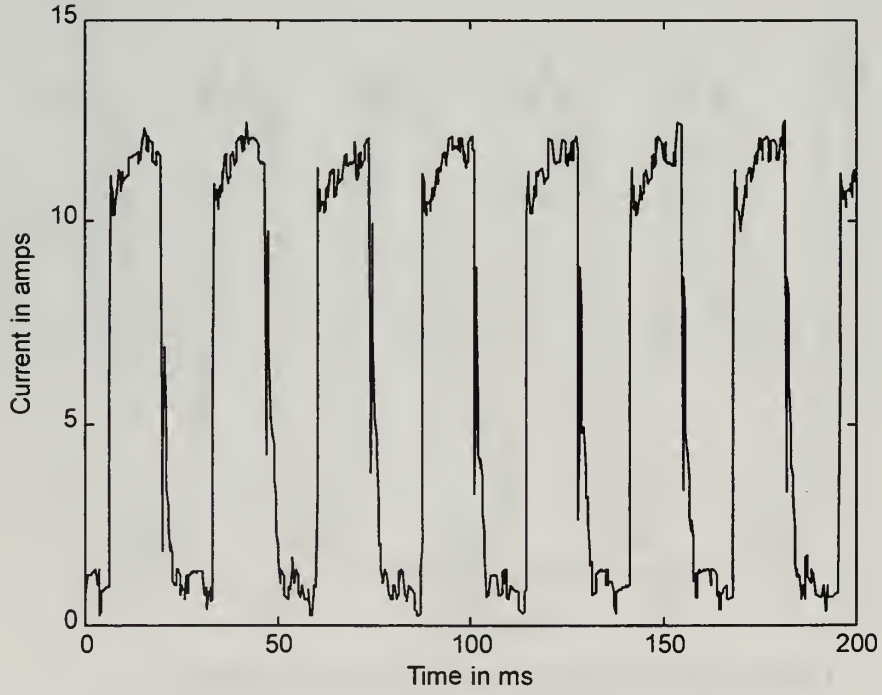

Figure 5-6f, Output Current Oscillogram, DC-DC4

6. Observations

These experiments verified two of the three phenomena identified in Series "A": bus voltage settling time decreasing with increased line inductance under a light source-side buck chopper load and the amplification of the noise at the output under an oscillating load condition. Two additional affects were also noted: The absence of load voltage overshoot under certain loading and inductance conditions and the introduction of bus noise under a non-synchronous double load oscillation.

E. TWO BUCK CHOPPERS FEEDING ONE BUCK CHOPPER

1. Device Noise Levels

When the source-side buck chopper outputs were placed in parallel, the noise level on the bus was increased. As stated before, the output noise level of the source-side buck choppers was approximately one percent while functioning under both light and heavy load conditions when operating autonomously. When the two source-side buck chopper outputs were tied to a common bus for operation, the noise level increased to approximately 12 percent (25 volts peak-to-peak) under light load conditions and approximately two percent (5 volts peak-to-peak) under heavy load conditions. This phenomena also translated into noise on the bus current level measurements.

The noise level under light source-side load conditions made the gathering of meaningful source-side buck chopper to load-side buck chopper bus current and voltage disturbance information impossible. The parameters of interest were masked in the noise. Although the bus noise precluded the gathering of data, the output of the load-side buck chopper was not effected. The noise under heavy source-side load conditions was

significantly higher than in the previous sections, but not large enough to completely mask the parameters of interest. The output characteristics of the load-side buck chopper were not effected by the bus noise; the noise levels remained consistent with the Series "A" experiments.

2. Light Load to Heavy Load

As stated above, when the devices were prepared for testing under a light source-side buck chopper loading, there was excessive noise, approximately 20 volts peak-to-peak, on the bus. This noise made the gathering of overshoot and settling time data impossible. An interesting observation was made when the load was changed. After the transient was introduced and the load-side buck chopper load went high, the noise level dropped dramatically to approximately five volts peak-to-peak. This phenomenon is related to the load sharing characteristics of the source-side buck choppers. With the load demand so low, the house curve built into the source-side buck chopper controllers does not change the output voltage level enough to force the devices to evenly share the load. Therefore one of the source-side buck choppers tends to dominate the pair and provide most of the current while the other keeps trying to come up to load and failing. This oscillation is transferred to the observed bus voltage and current levels. Before the transient, DC-DC1 was providing most of the current to the loads. After the step change, the source-side devices shared the load equally. This effect was consistent at all line inductance levels. These effects can be seen graphically in Figures (5-7a) through (5-7d).

At a heavily loaded condition on the source-side buck chopper, the significantly reduced bus noise levels made bus data acquisition possible. In these experiments, the

source-side buck choppers shared the load equally at all times. For these tests, the results were consistent with the data collected in Series "A" heavy source-side buck chopper load experiments (see Table (5-6)).

3. Heavy Load to Light Load

Noise levels again interfered with the gathering of data for the light source-side buck chopper load. In these five cases, before the transient is introduced, the bus voltage noise was approximately five volts peak-to-peak and the load sharing between the two source-side buck choppers was equal. After the transient, the noise increased to 25 volts peak-to-peak and one of the source-side buck choppers, DC-DC1, assumed the majority of the load. Again, the output performance characteristics of the load-side buck chopper were essentially unchanged from the Series "A" experiments.

Under the heavy source-side buck chopper load, as in the light to heavy load transition above, the bus voltage noise and source-side buck chopper load sharing characteristics were constant. As before, all monitored parameters were consistent with the Series "A" experiments. The results are documented in Table (5-7).

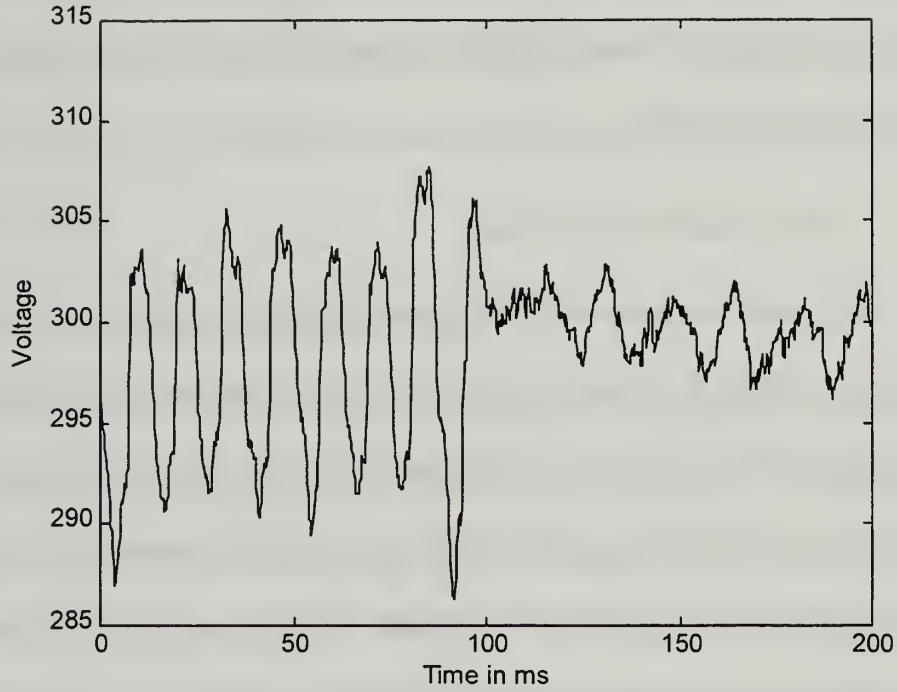

Figure 5-7a, Output Voltage Oscillogram, DC-DC1 / DC-DC2

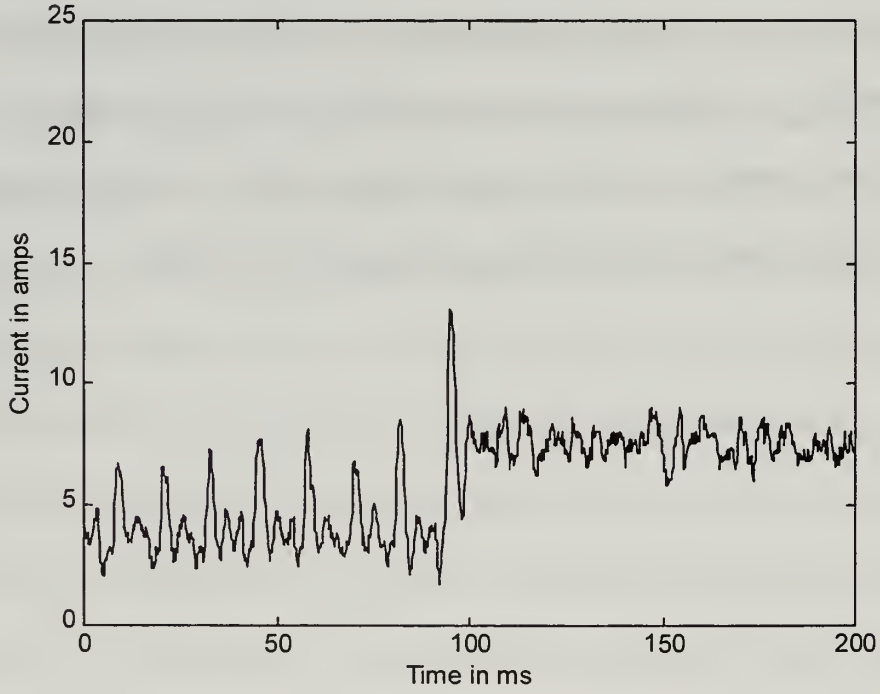

Figure 5-7b, Output Current Oscillogram, DC-DC1

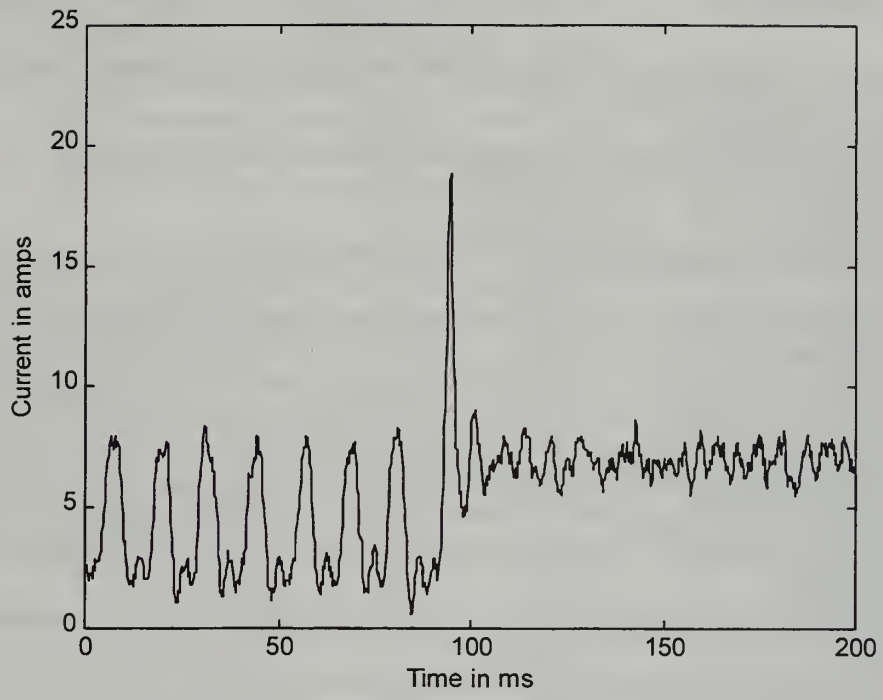

Figure 5-7c, Output Current Oscillogram, DC-DC2

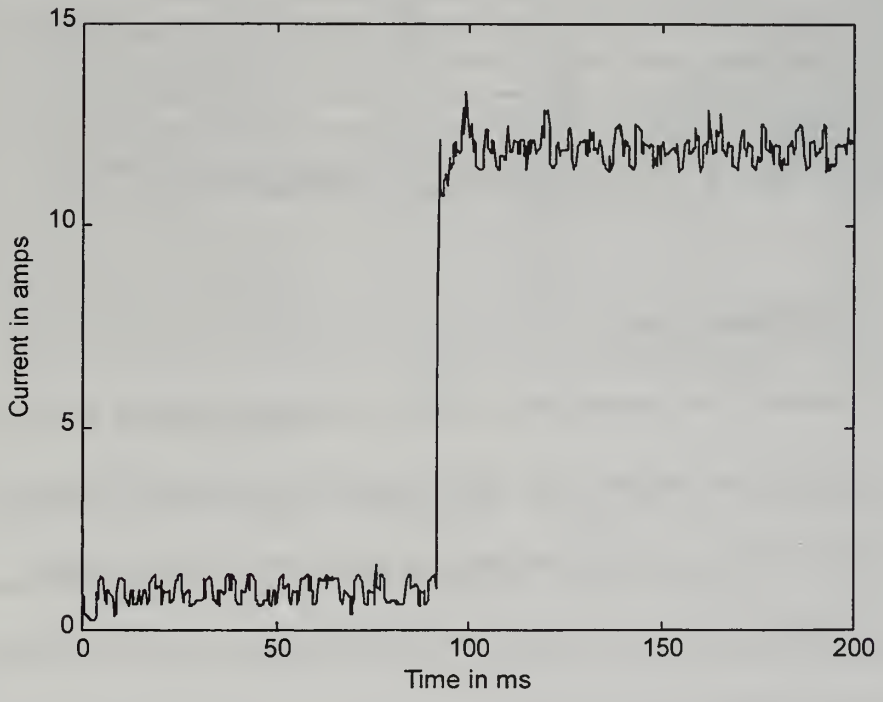

Figure 5-7d, Output Current Oscillogram, DC-DC3

PARAMETER	LIGHT LOAD ON SOURCE-SIDE DEVICES (C1-C5)	HEAVY LOAD ON SOURCE-SIDE DEVICE (C16-C20)
BUS CURRENT AT STEADY STATE	15.5 A	52.0 A
BUS CURRENT OVERSHOOT	noise	2.0 A
BUS CURRENT SETTLING TIME	noise	10 ms
BUS CURRENT NOISE LEVEL BEFORE TRANSIENT	4 A	1.0 A
BUS CURRENT NOISE LEVEL AFTER TRANSIENT	0.2 A	1.0 A
CURRENT SHARING BEFORE TRANSIENT (DC-DC1/DC-DC2)	≈ 90/10	50/50
CURRENT SHARING AFTER TRANSIENT (DC-DC1/DC-DC2)	≈ 50/50	50/50
BUS VOLTAGE AT STEADY STATE	300 V	299 V
BUS VOLTAGE OVERSHOOT	noise	5 V
BUS VOLTAGE SETTLING TIME	noise	20 ms
BUS VOLTAGE NOISE LEVEL BEFORE TRANSIENT	25 V	5 V
BUS VOLTAGE NOISE LEVEL AFTER TRANSIENT	5 V	5 V
LOAD CURRENT AT STEADY STATE	13.3 A	13.3 A
LOAD CURRENT OVERSHOOT	0.2 A	0.2 A
LOAD CURRENT SETTLING TIME	10 ms	10 ms
LOAD CURRENT NOISE LEVEL	0.2 A	0.2 A
LOAD VOLTAGE AT STEADY STATE	208	208
LOAD VOLTAGE SPIKE	8 V	9 V
LOAD VOLTAGE OVERSHOOT	5 V	5 V
LOAD VOLTAGE SETTLING TIME	10 ms	10 ms
LOAD VOLTAGE NOISE LEVEL	2 V	2 V

Table 5-6, Series C, Light to Heavy Load on Load-Side Buck Chopper

4. Oscillating Load

When the network was operated under a 50 Hz oscillating condition with a light load on the source-side buck choppers, bus voltage noise levels oscillated between five and 25 volts peak-to-peak, in sync with the changing load demand. Under a heavy source-side buck chopper load, the noise level was a uniform five volts. The load-side buck chopper output voltage peak-to-peak noise level was a consistent 25 volts under all source-side buck chopper load conditions. This was a slight variation from the Series

"A" data. Figures (5-8a) through (5-8e) are oscillograms demonstrating these effects for a light source-side buck chopper load level and 9.0 μH of line inductance.

PARAMETER	LIGHT LOAD ON SOURCE-SIDE DEVICES (C6-C10)	HEAVY LOAD ON SOURCE-SIDE DEVICE (C20-C25)
BUS CURRENT AT STEADY STATE	7.7 A	44 A
BUS CURRENT OVERSHOOT	noise	4.0 A
BUS CURRENT SETTLING TIME	noise	10 ms
BUS CURRENT NOISE LEVEL BEFORE TRANSIENT	0.2 A	1.0 A
BUS CURRENT NOISE LEVEL AFTER TRANSIENT	4 A	1.0 A
CURRENT SHARING BEFORE TRANSIENT (DC-DC1/DC-DC2)	≈ 50/50	50/50
CURRENT SHARING AFTER TRANSIENT (DC-DC1/DC-DC2)	≈ 90/10	50/50
BUS VOLTAGE AT STEADY STATE	300 V	300 V
BUS VOLTAGE OVERSHOOT	noise	5 V
BUS VOLTAGE SETTLING TIME	noise	20 ms
BUS VOLTAGE NOISE LEVEL BEFORE TRANSIENT	5 V	5 V
BUS VOLTAGE NOISE LEVEL AFTER TRANSIENT	25 V	5 V
LOAD CURRENT AT STEADY STATE	1.4 A	1.4 A
LOAD CURRENT OVERSHOOT	0.2 A	0.2 A
LOAD CURRENT SETTLING TIME	15 ms	15 ms
LOAD CURRENT NOISE LEVEL	0.2 A	0.2 A
LOAD VOLTAGE AT STEADY STATE	208	208
LOAD VOLTAGE SPIKE	10 V	9 V
LOAD VOLTAGE OVERSHOOT	6 V	5 V
LOAD VOLTAGE SETTLING TIME	15 ms	15 ms
LOAD VOLTAGE NOISE LEVEL	2 V	2 V

Table 5-7, Series C, Heavy to Light Load on Load-Side Buck Chopper

5. Observations

The primary effect observed in this series of experiments is that the bus voltage ripple was apparently caused by poor load sharing. When load demand on the two source-side buck choppers was greater than 15.5 amps, the two devices shared the load current equally and the bus voltage noise level was approximately two percent peak-to-peak. The next lowest source-side buck chopper load examined was approximately 7.7

amps (estimated from oscilloscope readings and verified by calculation), at this level the voltage ripple jumped to 15% peak-to-peak and there was a skewed load sharing profile between the source-side devices.

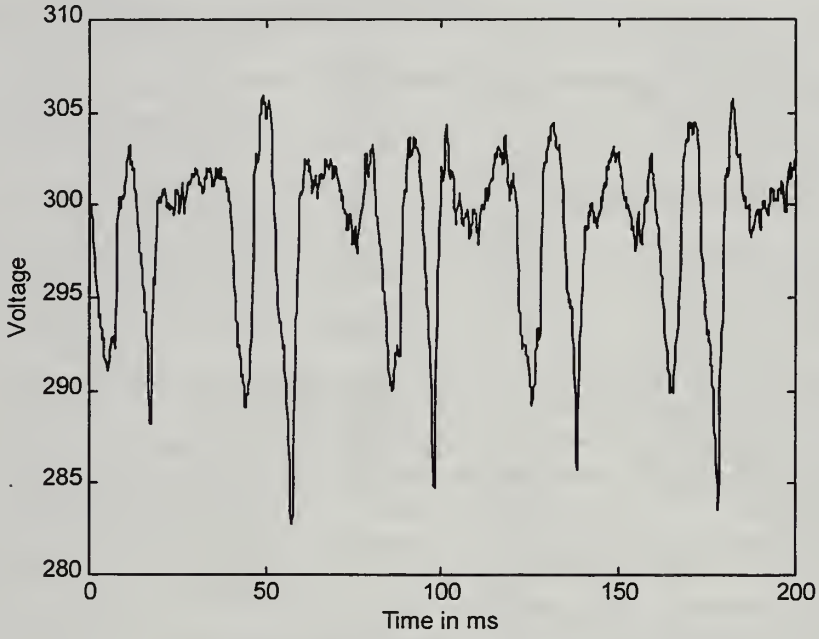

Figure 5-8a, Voltage Oscillogram

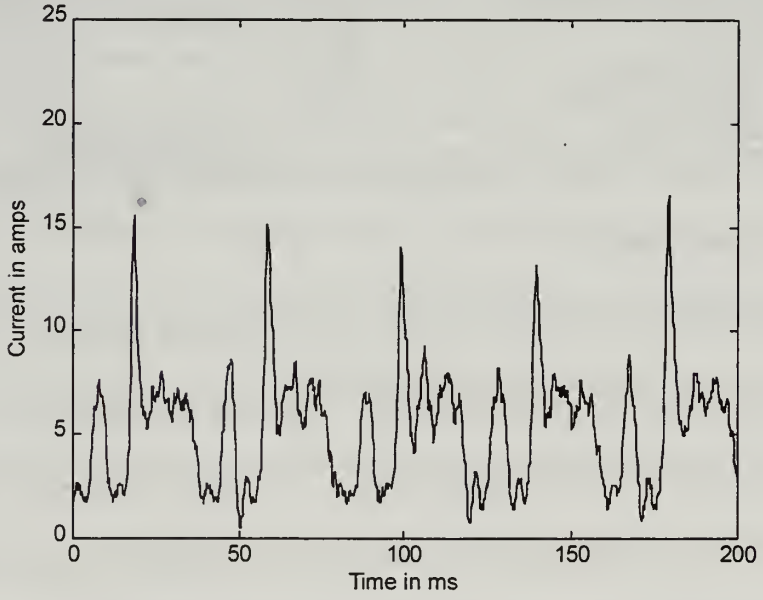

Figure 5-8b, Output Current Oscillogram, DC-DC1

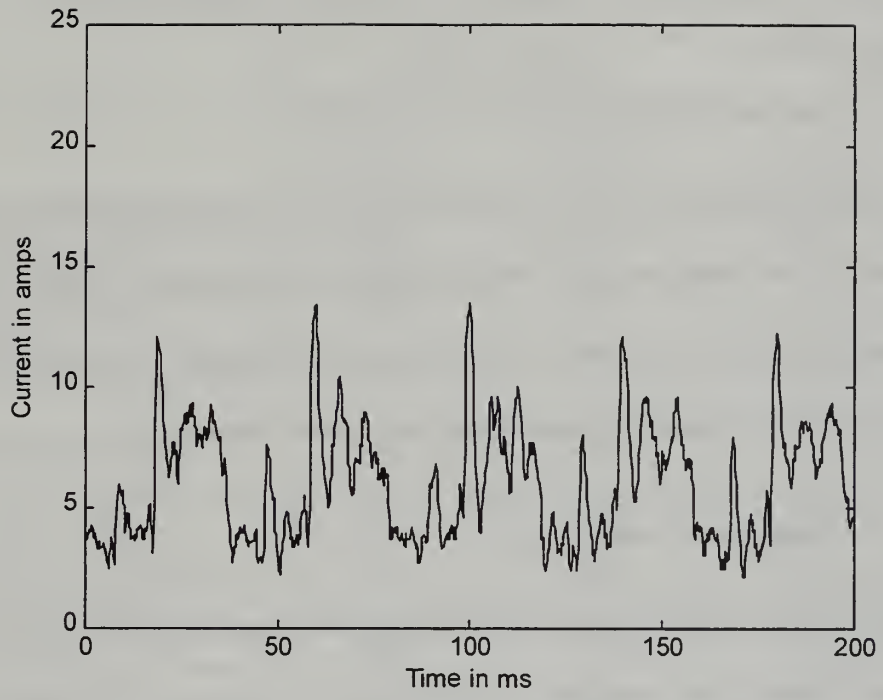

Figure 5-8c, Output Current Oscillogram, DC-DC2

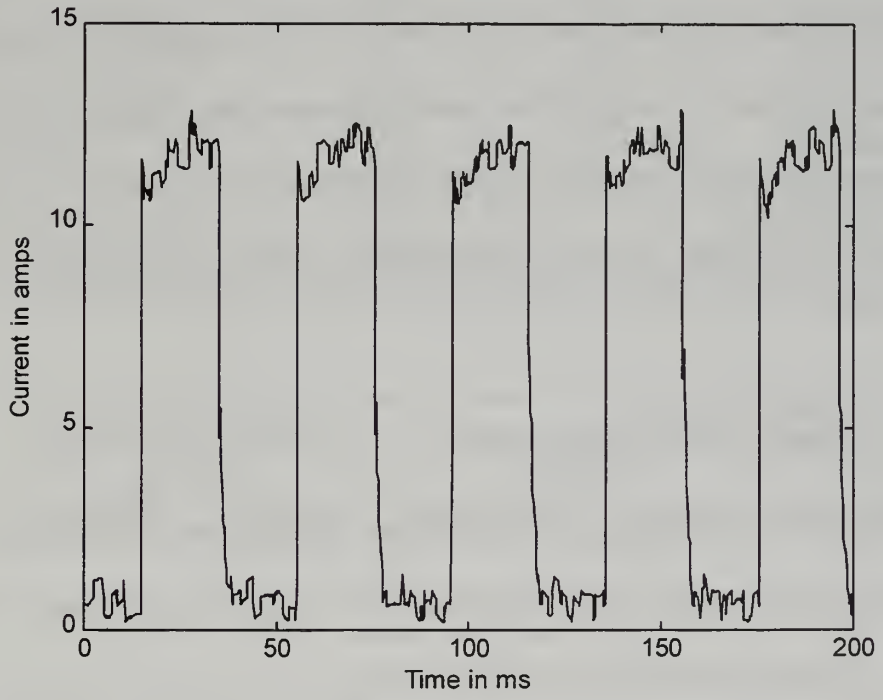

Figure 5-8d, Output Current Oscillogram, DC-DC3

F. TWO BUCK CHOPPERS FEEDING TWO BUCK CHOPPERS IN PARALLEL

1. Device Noise Levels

The voltage noise level on the bus during this series of experiments varied from as high as 15 percent under light source-side buck chopper load conditions to approximately two percent under heavier load demand. The load-side buck choppers, as in Series "B", exhibited a two percent voltage ripple throughout this series of experiments.

2. Light Load to Heavy Load

There were no new phenomena observed in this set of experiments. As in the Series "C" tests, voltage noise precluded the recording of meaningful source-side buck chopper to load-side buck chopper bus parameter data in the light source-side buck chopper load with a light static load. Under the other three load conditions, the noise levels subsided, paralleling the results of the Series "C" experiments. A similar load voltage overshoot/line inductance effect identified in the Series "B" experiments was also observed in these experiments. Table (5-8) summarizes the results of this set of experiments.

3. Heavy Load to Light Load

The results of these experiments were consistent at all load demands and line inductance levels. The data obtained was consistent with the previous experiments with a single variation. The line inductance/bus voltage settling time relationship observed in Series "A" and Series "B" was not observed. Table (5-9) documents the data gathered in these experiments.

PARAMETER	LIGHT LOAD ON SOURCE-SIDE DEVICE		HEAVY LOAD ON SOURCE-SIDE DEVICE	
	10% LOAD ON DC-DC4 (D1-D5)	90% LOAD ON DC-DC4 (D31-D35)	10% LOAD ON DC-DC4 (D16-D20)	90% LOAD ON DC-DC4 (D46-D50)
BUS CURRENT AT STEADY STATE	16.4 A	24.1 A	42.7 A	50.4 A
BUS CURRENT OVERSHOOT	noise	2.0 A	2.0 A	2.0 A
BUS CURRENT SETTLING TIME	noise	10 ms	10 ms	10 ms
BUS CURRENT NOISE LEVEL BEFORE TRANSIENT	4 A	0.2 A	0.2 A	0.2 A
BUS CURRENT NOISE LEVEL AFTER TRANSIENT	0.2 A	0.2 A	0.2 A	0.2 A
CURRENT SHARING BEFORE TRANSIENT (DC-DC1/DC-DC2)	≈ 90/10	50/50	50/50	50/50
CURRENT SHARING AFTER TRANSIENT (DC-DC1/DC-DC2)	50/50	50/50	50/50	50/50
BUS VOLTAGE AT STEADY STATE	299 V	299 V	298 V	298 V
BUS VOLTAGE OVERSHOOT	noise	4 V	4 V	4 V
BUS VOLTAGE SETTLING TIME	noise	20 ms	15 ms	20 ms
BUS VOLTAGE NOISE LEVEL BEFORE TRANSIENT	25 V	5 V	5 V	5 V
BUS VOLTAGE NOISE LEVEL AFTER TRANSIENT	5 V	5 V	5 V	5 V
LOAD CURRENT AT STEADY STATE	13.3 A	13.3 A	13.3 A	13.3 A
LOAD CURRENT OVERSHOOT	0.1 A	0.1 A	0.1 A	0.1 A
LOAD CURRENT SETTLING TIME	10 ms	5 ms	5 ms	5 ms
LOAD CURRENT NOISE LEVEL	0.1 A	0.1 A	0.1 A	0.1 A
LOAD VOLTAGE AT STEADY STATE	208 V	208 V	208 V	208 V
LOAD VOLTAGE SPIKE	10 V	10 V	10 V	10 V
LOAD VOLTAGE OVERSHOOT	3 V	See Table 5-8a		
LOAD VOLTAGE SETTLING TIME	5 ms	See Table 5-8a		
LOAD VOLTAGE NOISE LEVEL	4 V	4 V	4 V	4 V

Table 5-8, Series D, Light to Heavy Load on Load-Side Buck Chopper

	LIGHT LOAD ON DC-DC1		HEAVY LOAD ON DC-DC1			
	HEAVY LOAD ON DC-DC4 (D16-D20)		LIGHT LOAD ON DC-DC4 (D31-D35)		HEAVY LOAD ON DC-DC4 (D46-D50)	
LINE INDUCTANCE - μH	OVERSHOOT - V	SETTLING TIME - ms	OVERSHOOT - V	SETTLING TIME - ms	OVERSHOOT - V	SETTLING TIME - ms
0.0	5	15	5	15	5	15
4.5	0	5	5	10	0	5
9.0	0	5	0	5	0	5
13.5	0	5	0	5	0	5
18.0	0	5	0	5	0	5

Table 5-8a, Line Inductance - Load Voltage Overshoot/Settling Time Relationship

PARAMETER	LIGHT LOAD ON SOURCE-SIDE DEVICE		HEAVY LOAD ON SOURCE-SIDE DEVICE	
	10% LOAD ON DC-DC4 (D1-D5)	90% LOAD ON DC-DC4 (D31-D35)	10% LOAD ON DC-DC4 (D16-D20)	90% LOAD ON DC-DC4 (D46-D50)
BUS CURRENT AT STEADY STATE	8.7 A	16.4 A	35 A	42.7 A
BUS CURRENT OVERSHOOT	noise	1.0 A	1.0 A	1.0 A
BUS CURRENT SETTLING TIME	noise	10 ms	10 ms	10 ms
BUS CURRENT NOISE LEVEL BEFORE TRANSIENT	4 A	0.2 A	0.2 A	0.2 A
BUS CURRENT NOISE LEVEL AFTER TRANSIENT	0.2 A	0.2 A	0.2 A	0.2 A
CURRENT SHARING BEFORE TRANSIENT (DC-DC1/DC-DC2)	50/50	50/50	50/50	50/50
CURRENT SHARING AFTER TRANSIENT (DC-DC1/DC-DC2)	≈ 90/10	50/50	50/50	50/50
BUS VOLTAGE AT STEADY STATE	300 V	300 V	301 V	301 V
BUS VOLTAGE OVERSHOOT	noise	4 V	4 V	4 V
BUS VOLTAGE SETTLING TIME	noise	20 ms	15 ms	20 ms
BUS VOLTAGE NOISE LEVEL BEFORE TRANSIENT	5 V	5 V	5 V	5 V
BUS VOLTAGE NOISE LEVEL AFTER TRANSIENT	25 V	5 V	5 V	5 V
LOAD CURRENT AT STEADY STATE	1.5 A	1.5 A	1.5 A	1.5 A
LOAD CURRENT OVERSHOOT	0.1 A	0.1 A	0.1 A	0.1 A
LOAD CURRENT SETTLING TIME	5 ms	5 ms	5 ms	5 ms
LOAD CURRENT NOISE LEVEL	0.1 A	0.1 A	0.1 A	0.1 A
LOAD VOLTAGE AT STEADY STATE	208 V	208 V	208 V	208 V
LOAD VOLTAGE SPIKE	10 V	10 V	10 V	10 V
LOAD VOLTAGE OVERSHOOT	5 V	5 V	5 V	5 V
LOAD VOLTAGE SETTLING TIME	15 ms	15 ms	15 ms	15 ms
LOAD VOLTAGE NOISE LEVEL	4 V	4 V	4 V	4 V

Table 5-9, Series D, Heavy to Light Load on Load-Side Buck Chopper

4. Oscillating Load

As in Series "B", the results for a single load-side buck chopper supplying an oscillating load were consistent with the previous experiments. The peak-to-peak voltage noise was 20 volts under a light source-side converter load conditions and 25 volts under a heavy load conditions. The double oscillating load produced large ripples in the bus current and voltage as well as in both load-side buck chopper outputs. The source-side

buck chopper(s) output voltage assumed a 10 volt peak-to-peak ripple as in the Series "B" experiments. The bus current ripple was approximately eight amps peak-to-peak , a lower level than observed in Series "B". The 75 Hz load again displayed a 50 volt peak-to-peak ripple and the 50 Hz load produced in a 20 volt ripple as before.

5. Observations

No new phenomena were uncovered in these experiments, but several previously observed effects were confirmed. Two of these effects are more significant for future design of DC distribution networks. The source-side buck chopper load sharing relationship to bus voltage and current noise identified in Series "C" was confirmed. Also the reduction in the load voltage overshoot level at higher source-side buck chopper load and inductance conditions seen in Series "B" was verified.

G. PEBB TESTBED

The PEBB testbed functioned as designed throughout the testing. The quick and easy reconfiguration capability was instrumental in the performance of these experiments. The functionality and utility of the testbed was found to be excellent.

VI. CONCLUSIONS

A. SUMMARY OF RESULTS

As indicated by the steady-state and transient performance data collected in this research effort, a system of networked buck converters may be successfully used to provide DC power in a DC ZEDS architecture. In particular, the buck converters were found to operate stably and the transient response figures of merit were in specification when connected in the four topologies investigated in this project: two converters series connected, a high-power device feeding two low-power devices, two high-power devices operating in parallel feeding a single, low-power device, and two-high power devices operating in parallel feeding two low-power devices off of a common bus. Design considerations need to be made to account for the non-ideal nature of parallel-output devices as well as the effect of high-power, high-frequency transients in the network.

1. Networking of Buck Choppers

When buck choppers are interconnected, noise is introduced into the network. Aside from the normal effects of electromagnetic interference (EMI) and radio frequency interference (RFI) experienced in measurements, there are several possible sources for this noise. Switching effects, harmonics, and mismatched components all contribute to the noise levels observed. These effects are present both when the outputs of multiple source-side devices or the inputs of load-side devices are tied to a common bus. In this research, values ranging from one percent ripple for the series connection, to 15 percent ripple for the parallel connected source-side buck choppers under a light load, were

observed. No other adverse effects are observed when buck choppers are operated in a network.

2. Source-Side Buck Chopper Load Sharing

When two or more source-side buck choppers are configured to provide power to a single bus, the load sharing characteristics are paramount. When the load demand on the source-side buck choppers falls below a threshold, approximately 25 % of the total rated capacity, the devices do not share the load equally and appreciable harmonics appear on the bus. When the load demand was above the threshold, the bus noise levels were attenuated to a level of five volts, peak-to-peak. Based on the data obtained in this endeavor, a load requirement of 25% of the total capacity of the paralleled units is required for proper load sharing between the source-side buck choppers employing the algorithm described in Chapter III.

3. Effect of Line Inductance

The general trend observed in this research was that increased line inductance between source-side and load-side buck choppers tended to slightly reduce the settling times in the network when a transient was introduced. Under light source-side buck chopper loading, the bus voltage settling time is reduced as line inductance is increased. This effect is most likely caused by the line inductance slowing the change in current level on the bus, thereby reducing the amount of voltage and current overshoot. Since the overshoot levels were significantly higher when the source-side buck choppers were lightly loaded, the relationship between the settling time and the line inductance is most

noticeable under these conditions. This phenomena was only observed when a single source-side buck chopper was connected to the network, noise levels on the bus masked this information when the source-side buck choppers were placed in parallel.

In experiments involving two load-side buck choppers, the load-side output voltage overshoot and the associated settling time were reduced as line inductance between the source-side and load-side buck choppers was increased. The common factor in these experiments was the level of current flowing through the RL Links. As more current passed through the links, the load-side output voltage overshoot reduced to a non-detectable level. This effect was most likely caused by the RL links retarding the effect of the transient on the bus, allowing the controller to reach steady state without any observable overshoot. The overall effect of introducing line inductance into the network was minimal, and in the areas where effects were observed, the effect tended to be beneficial to the overall operation.

B. RECOMMENDATIONS FOR AREAS OF FUTURE STUDY

As stated in the abstract, the DC ZEDS concept broaches a multitude of technical questions. Based on this research endeavor, the following areas are suggested as topics for further study.

1. Transient Response

In this research, figures of merit of the transient response of the network were investigated for a particular algorithm and set of control gains. As such, it provides important preliminary validation of the interconnection of the system components and

documents base values of settling time, overshoot and harmonics. In particular, the interaction of line inductance, load levels and control algorithms should provide valuable information for use in practical design and system optimization. A more detailed study of various control schemes and gains as well as different converter components should be considered a research priority.

2. Inclusion of ARCPs

This project focused on the buck chopper, SSCM, as the primary test device. But the DC ZEDS concept also includes inverters, SSIMs. Although some of the information developed here can be extrapolated into an ARCP architecture, the behavior of ARCPs in a DC ZEDS network must be investigated. As the hardware is now available at the Naval Postgraduate School, closed-loop control algorithms may be designed and the units integrated in with the buck choppers. The additional harmonics and controller interactions should provide interesting dynamics and introduce several issues for investigation.

3. Inductive Loads

All experiments performed in this project used pure resistive DC loads, but most actual shipboard electrical loads are AC and both resistive and inductive in nature. The effect on the devices, controllers, and the network in general needs to be studied. This would be the next logical extension of this research.

4. Parallel Operation of Source-Side Buck Choppers (SSCM #1)

A significant increase in the output noise level was observed when the source-side buck choppers were configured with parallel outputs. Even though the noise level observed is relatively small as compared to the DC voltage level under a proper load sharing condition, a technique to minimize this effect needs to be explored.

5. Resonant DC-DC Converters

The devices studied in this project were hard-switched buck choppers. Resonant converters, possessing a considerable advantage in efficiency, could be employed to greatly reduce the switching losses in, as well as the physical size of, the buck converters. Modification of the DC ZEDS architecture to exploit this characteristic could pay enormous dividends, especially at higher power levels.

C. SUMMATION

This research is closely related to ongoing work at NPS and other educational institutions in support of the Naval Surface Warfare Center, Carderock Division. In the execution of this research effort several major accomplishments were realized.

- The PEBB Testbed for modeling a DC ZEDS was designed, built and tested.
- SSCMs (Source and load-side buck choppers) built in support of previous research were integrated into the testbed and validated.
- Methodology for investigating the effects of interconnecting the SSCMs was developed and executed.
- The results of these investigations were documented for future use.

The PEBB Testbed was a central feature of this research. It was found to be an important tool in the analysis and development of a DC Zonal Electrical Distribution System.

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   Monterey, CA 93943-5121

10. Robert W. Ashton, Code EC/Ah 1
    Department of Electrical and Computer Engineering
    Naval Postgraduate School
    Monterey, CA 93943-5121

11. Thomas L. Langlois 2
c/o Floyd T. Langlois
136 Woodstock
Conroe, TX 77302